## EE434

## ASIC and Digital Systems

## Midterm Exam 1

Mar. 4, 2020. (2:10pm - 3pm)
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Name:
WSU ID:

| Problem | Points |  |
| :---: | :---: | :--- |
| 1 | 10 |  |
| 2 | 10 |  |
| 3 | 10 |  |
| 4 | 10 |  |
| 5 | 10 |  |
| 6 | 10 |  |
| 7 | 10 |  |
| 8 | 10 |  |
| Total | 80 |  |

## Problem \#1 (Static CMOS gates, 10 points)

Design the following logic using the static CMOS design methodology. Try to minimize the \# transistors. Available input: $A, B, C, D$.

$$
Y=\overline{A+\bar{B} \cdot \bar{C} \cdot \bar{D}}
$$

## Problem \#2 (Static CMOS gates, 10 points)

Design the following logic using the static CMOS design methodology. Try to minimize the \# transistors. Available input: $A, B, C, D$.

$$
Y=A \cdot B \cdot(\bar{C}+\bar{D})
$$

## Problem \#3 (Static CMOS gates, 10 points)

The following shows the NFET network of a static CMOS gate. Express the output $Y$ as a Boolean function of the inputs $(A \sim F)$. (You don't need to simplify the expression.)


## Problem \#4 (Static CMOS gates, 10 points)

The following shows the PFET network of a static CMOS gate. Express the output $Y$ as a Boolean function of the inputs $(A \sim E)$. (You don't need to simplify the expression.)


## Problem \#5 (Transmission Gates, 10 points)

Design (draw a schematic) the following Boolean function using transmission gates only.

$$
Y=A \oplus(B \cdot(C \oplus D))
$$

Available inputs: $A, B, C, D, 0,1$. Use the following symbols for the transmission gates.

(\# TGs $\leq 12: 10$ points. $13 \leq \# ~ T G s \leq 15: 7$ points. $16 \leq \# T G s \leq 18: 5$ points. \# TGs>18: 3 points)

## Problem \#6 (Sequential Logic, 10 points)

The following truth table shows the function of a sequential logic. CK is the clock signal. A, B, D, E, and F are data or control (e.g., reset) signals. What does the gate do?? Explain the function in detail.

| A | B | D | E | F | CK | $\mathrm{Q}^{+}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0 | X | 0 | E | X | $\downarrow$ | E |
| 0 | X | 1 | X | F | $\downarrow$ | F |
| 1 | B | X | X | X | $\downarrow$ | B |
| X | X | X | X | X | $\uparrow$ | Q |
| X | X | X | X | X | 0 or 1 | Q |

## Problem \#7 (Analysis, 10 points)

What do the following circuits do? (You can ignore the numbers in the schematics.) For each schematic, you can draw a truth table or express the output as a function of the inputs.

(JSSC'97)

(JSSC'96)

Problem \#8 (Sequential Logic, 10 points)
Explain the function of the following logic. CK: Clock. D, E: Data and/or control input.


