EE466

ASIC and Digital Systems

Final Exam

Dec. 13, 2017. (1pm – 3pm)

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Name:

WSU ID:

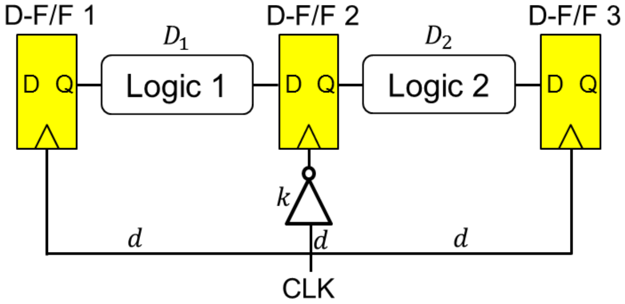
Problem	Points	
1	20	
2	30	
3	20	
4	20	
5	20	
6	20	
Total	130	

* Allowed: Textbooks, cheat sheets, class notes, notebooks, calculators, watches

* Not allowed: Electronic devices (smart phones, tablet PCs, laptops, etc.) except calculators and watches

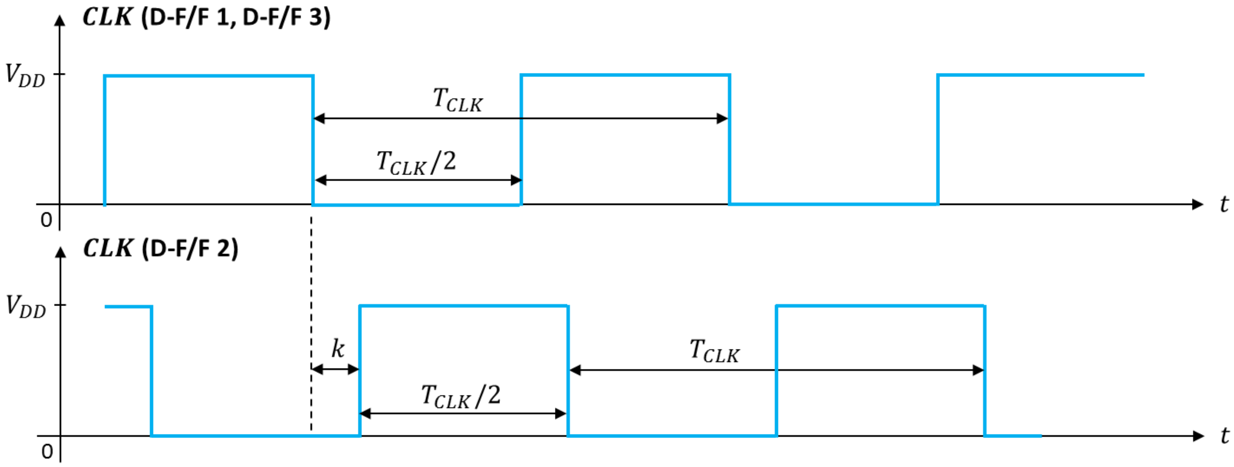
Problem #1 (Timing Analysis, 20 points)

The following shows a system consisting of two D-F/Fs and two logic stages (Logic 1 and Logic 2).



- D_n: Delay of Logic n
- d: Delay from the clock source to D-F/F 1 and the input of the inverter
- k: Delay of the inverter ($\boldsymbol{0 < k < T_{CLK}/4}$)
- T_{CLK}: Clock period
- T_s: Setup time
- T_h: Hold time
- T_{CQ}: Clk-to-Q delay of a D-F/F
- Clock duty cycle: 50%

The following shows the waveforms of the clock at the clock input of D-F/F 1 and D-F/F 2 for better understanding.

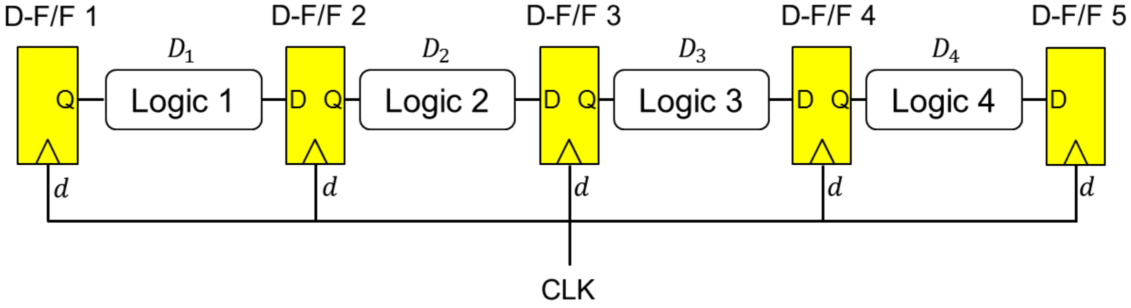


1) Does the circuit have any setup time constraints? If yes, find all setup-time constraints (inequalities) for the system. If no, prove that the circuit does not have any setup time constraints (10 points).

2) Does the circuit have any hold time constraints? If yes, find all hold-time constraints (inequalities) for the system. If no, prove that the circuit does not have any hold time constraints (10 points).

Problem #2 (Timing Analysis, 30 points)

The following shows a pipelined logic. All the F/Fs are identical, i.e., they have the same setup time, hold time, and T_{CQ}.



The following shows the constants used in this problem.

- T_s: Setup time of a D-F/F
- T_h: Hold time of a D-F/F
- T_{CQ}: Clk-to-Q delay of a D-F/F
- D_n: Delay of Logic n
- T_{CLK}: Clock period
- d: Delay from the clock source to each D F/F.

The setup time constraint for Logic n is as follows:

$$d + T_{CQ} + D_n \leq d + T_{CLK} - T_s$$

If the delay of Logic 1 (D_1) is too large (i.e., $D_1 > T_{CLK} - T_S - T_{CQ}$), it violates the setup time constraint of Logic 1. In this case, we can intentionally apply clock skew to the system so that Logic 1 has a more loose setup time constraint while some of the other logic stages have tighter setup time constraints. This method is called "useful skew".

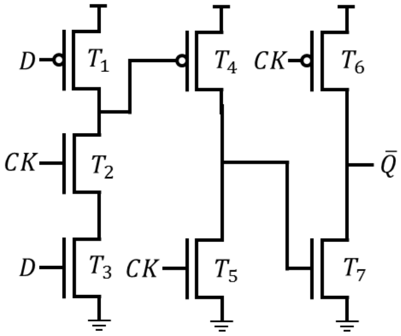
We compare the following three methods for the useful skew.

1) We apply clock skew to D-F/F 2 only. In this case, the delay from the clock source to D-F/F 2 becomes $d + \alpha$ where α is positive. Assume $D_2 < T_{CLK} - T_S - T_{CQ}$. Find the range (minimum and maximum) of α, i.e., represent the minimum and the maximum values of α as functions of the constants listed above (5 points).

2) We apply the same clock skew to D-F/F 2, D-F/F 3, D-F/F 4, and D-F/F 5. In this case, the delay from the clock source to the four D-F/Fs (D-F/F 2, 3, 4, 5) becomes $d + \beta$ where β is positive. Assume $D_n < T_{CLK} - T_S - T_{CQ}$ for $n = 2,3,4,5$. Find the minimum and the maximum values of β, i.e., represent the minimum and the maximum values of β as functions of the constants listed above (10 points).

3) We apply different clock skews to D-F/F 2, D-F/F 3, D-F/F 4, and D-F/F 5. In this case, the delay from the clock source to D-F/F m (where $m = 2,3,4,5$) becomes $d + \Delta_m$ where Δ_m is positive and Δ_5 is given ($\Delta_5 + T_{CLK} - T_s - T_{CQ} - D_4 > 0$). Find the minimum and the maximum values of Δ_2, i.e., represent the minimum and the maximum values of Δ_2 as functions of the constants listed above ($T_s, T_h, T_{CQ}, D_1, D_2, D_3, D_4, T_{CLK}, \Delta_5$) (15 points).

Problem #3 (Sequential Logic & Transistor Sizing, 20 points)



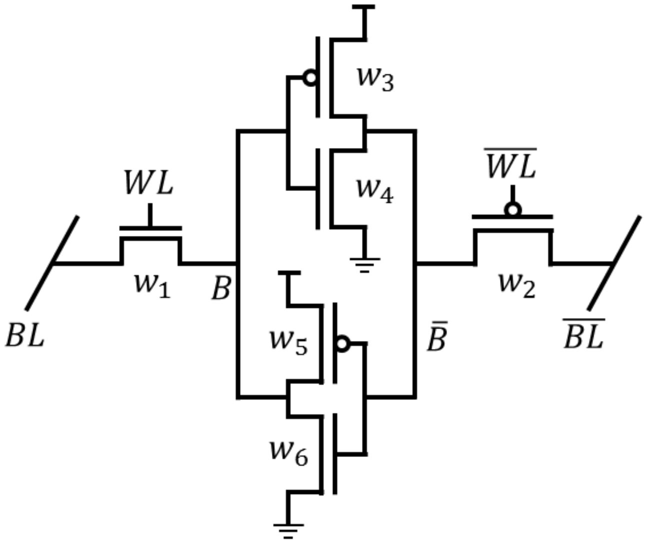
<Chang, JSSC'96>

The above figure shows a negative edge-triggered D-F/F: However, some of the transistors should be properly sized, otherwise it won't work correctly. Find all inequalities and/or equations required to guarantee that the circuit shown above works as a negative edge-triggered D-F/F. Use the following variables/constants. (Do not care about the sampling frequency, i.e., the clock period is sufficiently long).

- D: Data input of the F/F
- CK: Clock input
- $\bar{Q}$: Inverted data output
- R_m: ON resistance of transistor T_m
- V_{DD}: Supply voltage
- V_{tn}: Threshold voltage of a NFET
- V_{tp}: Threshold voltage of a PFET
- If $\bar{Q}$ is driven by a ratioed logic, $\bar{Q}$ should be less than or equal to $0.1V_{DD}$ for logical output 0 and greater than or equal to $0.9V_{DD}$ for logical output 1.
- If a node is floating, assume that the node holds its previous value (no leakage).

Problem #4 (Memory, 20 points)

The following figure shows a 6T SRAM cell. However, it uses an NFET and a PFET for the access transistors as shown in the figure. The wordline (WL) is set to 1 to access the cell and 0 to forbid accessing the cell. Notice that $\overline{WL}$ is connected to the gate of the PFET access transistor. The length of each TR is set to the minimum length l.



Assume that $B = 0$ ($\bar{B} = 1$) is stored in the SRAM cell. Derive all inequalities and/or equations for the widths of the six transistors to write 1 to the SRAM cell (in this case, BL and $\overline{BL}$ are set to 1 and 0, respectively, and WL and $\overline{WL}$ are set to 1 and 0, respectively, to access the cell and write 1 into the cell). Use the following variables/constants.

- w_m: The width of the transistor w_m
- V_{DD}: Supply voltage
- V_{tn}: Threshold voltage of an NFET
- V_{tp}: Threshold voltage of a PFET

Note: You can use the transistor current formula or the voltage-divider formula. You don’t need to simplify the inequalities or equations, but you should mention exactly what conditions should be satisfied to be able to write 1 to the SRAM cell.

Problem #5 (Carry Look-Ahead Adder, 20 points)

The max. fanout is 4. The delay of an AND (OR) gate is Δ and the delay of a two-level (sum-of-product) logic is 2Δ. We are designing a 1024-bit carry look-ahead adder.

1) Represent c_{62} hierarchically using group-generated and group-propagated carries ($g_{i\cdot k}$, $p_{i\cdot k}$) and c_0 (primary carry-in), then compute the delay to compute c_{62} assuming all the primary input signals are available at time 0 (10 points).

2) Represent c_{827} hierarchically using group-generated and group-propagated carries ($g_{i:k}$, $p_{i:k}$) and c_0 (primary carry-in), then compute the delay to compute c_{827} assuming all the primary input signals are available at time 0 (10 points).

Problem #6 (Prefix Adder, 20 points)

The delay of an AND (OR) gate is Δ and the delay of a two-level (sum-of-product) logic is 2Δ. We are designing a 1024-bit Kogge-Stone adder.

1) Represent c_{52} hierarchically using group-generated and group-propagated carries ($g_{i \cdot k}$, $p_{i \cdot k}$) and c_0 (primary carry-in), then compute the delay to compute c_{52} assuming all the primary input signals are available at time 0 (10 points).

2) Represent c_{987} hierarchically using group-generated and group-propagated carries ($g_{i \cdot k}$, $p_{i \cdot k}$) and c_0 (primary carry-in), then compute the delay to compute c_{987} assuming all the primary input signals are available at time 0 (10 points).