EE46

VLSI System Design

Midterm Exam

Oct. 23, 2017. (12:10pm – 1pm)

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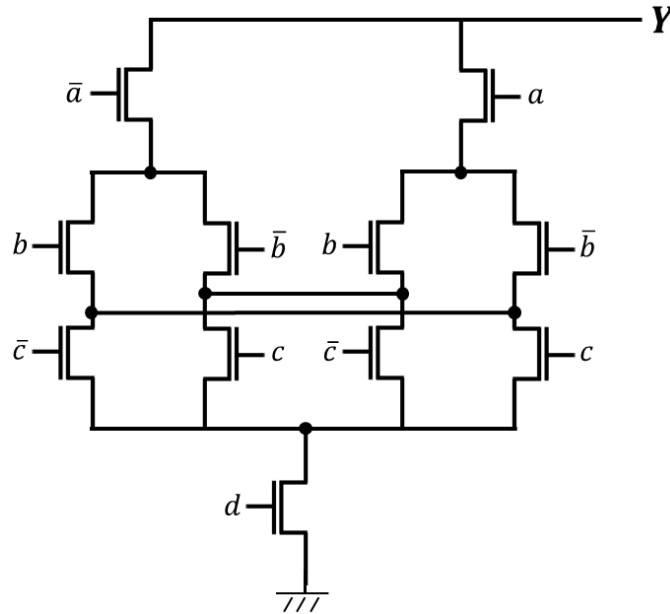
Name:

WSU ID:

Problem	Points	
1	10	
2	10	
3	10	
4	10	
5	10	
Total	50	

* Allowed: Textbooks, cheat sheets, class notes, notebooks, calculators, watches

* Not allowed: Electronic devices (smart phones, tablet PCs, laptops, etc.) except calculators and watches

Problem #1 (Static CMOS gates, 10 points).

The following schematic shows the nFET network of a static CMOS gate.
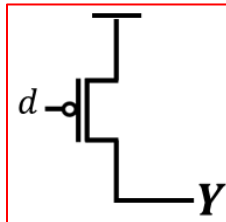

1) Express Y as a Boolean function of a, b, c and d. Simplify Y as much as possible.

$$Y = \overline{a(bcd + b\bar{c}d + \bar{b}cd + \bar{b}\bar{c}d) + \bar{a}(b\bar{c}d + bcd + \bar{b}cd + \bar{b}\bar{c}d)}$$

$$= \overline{a(bd + \bar{b}d) + \bar{a}(bd + \bar{b}d)} = \overline{bd + \bar{b}d} = \bar{d}$$

2) Draw a schematic for the pFET network of the gate.

Problem #2 (DC Analysis, 10 points).

The following shows the schematic of a tri-state inverter ($V_{out} = V_A \cdot \overline{V_{in}} + \overline{V_A} \cdot Z$).
$V_{tn} = |V_{tp}| = 0.2V$. $V_{DD} = 1V$. For the inverter, you can assume $V_{IL} = 0.45V$, $V_{OL} = 0V$, $V_{IH} = 0.55V$, $V_{OH} = 1V$, $V_M = 0.5V$. You don't need to show operation modes (cut-off, linear, saturation) in each region, but you should show some important values in the x- and y-axes.
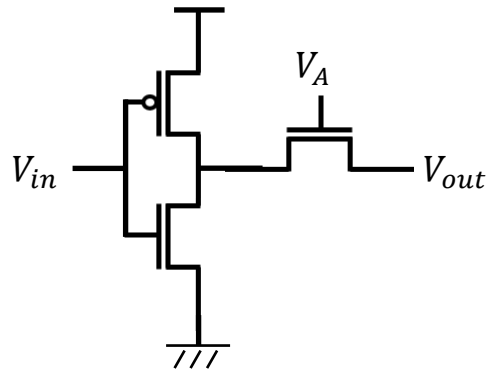
1) Draw a DC characteristic curve (V_{in} vs. V_{out}) when $V_A = 1V$.
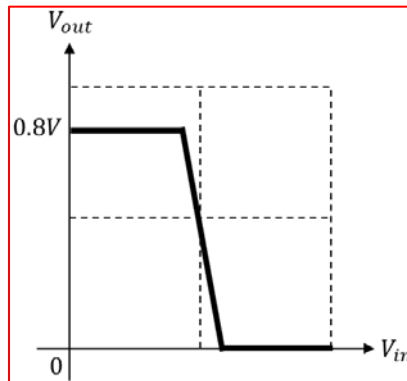
2) Draw a DC characteristic curve (V_{in} vs. V_{out}) when $V_A = 0.7V$.
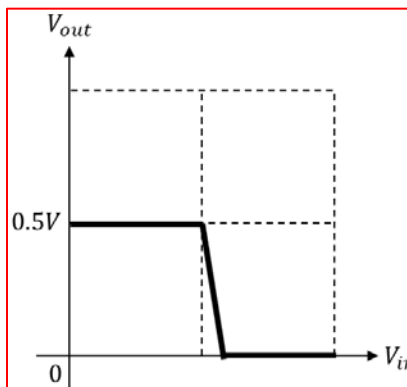
Problem #3 (Transistor Sizing, 10 points).

Size the transistors in the following pull-down network of a static CMOS gate. R_n is the resistance of a 1X NMOS transistor. C_L is the load cap. Ignore parasitic capacitances. Target time constant: $\tau = R_n \cdot C_L$. Try to minimize the total area.
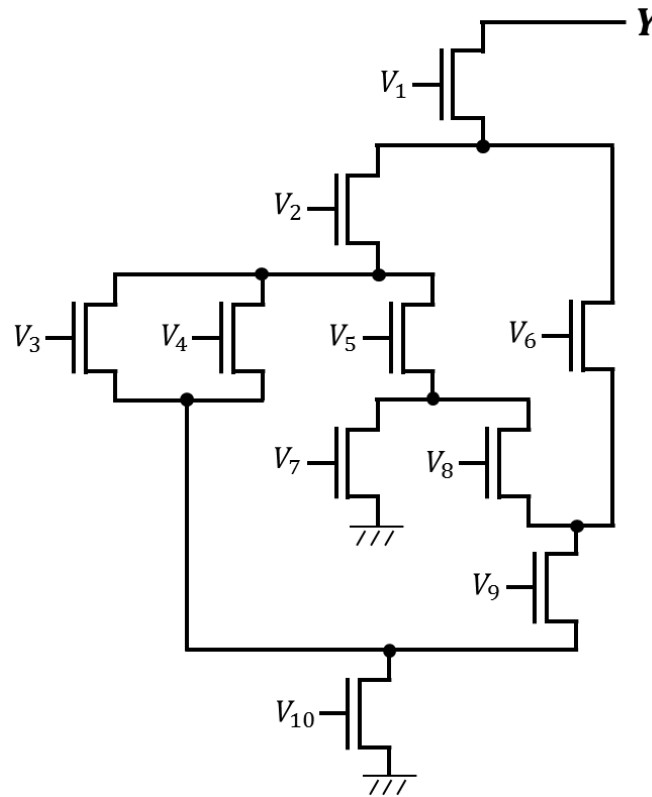
V_1: 6X
V_2: 6X
V_3: 2X
V_4: 2X
V_5: 6X
V_6: 2X
V_7: 2X
V_8: 6X
V_9: 6X
V_{10}: 6X

Problem #4 (Domino Logic, 10 points).

The following shows a four-stage domino logic. Input: $V_{1,1} \sim V_{4,d}$. Output: Y. Clock: CK.
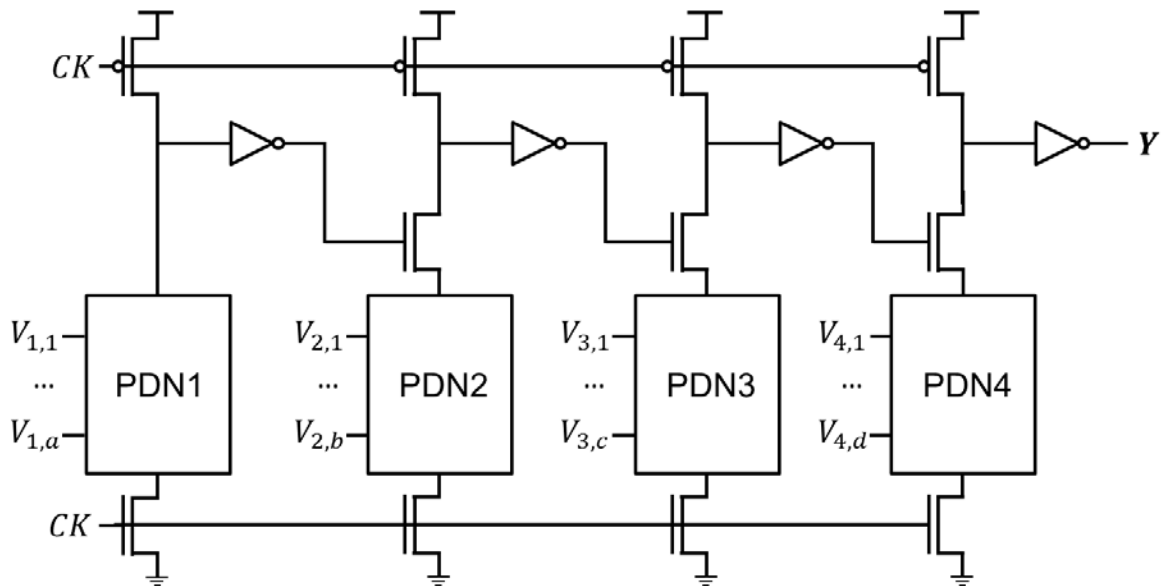

All the inputs are available at time 0 (i.e., the inputs are stable from time 0 until the end of the evaluation). The clock switches from high to low at time 0 for pre-charging and switches from low back to high at time t_1 for evaluation.

Does this domino logic have charge sharing problems? If your answer is yes, explain when it happens (or you can show an example). If your answer is no, explain or prove why it does not happen.

Charge sharing occurs.

Problem #5 (Sequential Logic, 10 points).

Design (draw a transistor-level schematic) a D Latch. The following shows the spec of the D latch.

- Input: D (data), S (set), R (reset)
- Output: Q
- Clock: CK
- Polarity: Positive (i.e., If $CK = 1$, Q follows D. If $CK = 0$, Q holds the previous value).
- Set
  - If $S = 1$, Q is always 1 no matter what D, R, and CK are.
  - If $S = 0$, we check R as follows.
- Reset
  - If $S = 0$ and $R = 1$
    - If $CK = 1$, Q is zero.
    - If $CK = 0$, Q holds the previous value.
  - If $S = 0$ and $R = 0$ (then, this is just a regular D Latch).
    - If $CK = 1$, Q follows D.
    - If $CK = 0$, Q holds the previous value.
- You can use gate-level symbols for inverters, NAND and NOR gates, and AND and OR gates (i.e., if you want to use these gates in your design, you can just draw gate-level symbols such as ▷∘ to simplify your schematic. However, for the body of the D Latch, use transistor symbols).