## EE466

## VLSI Design

Final Exam
Dec. 13, 2019. (3:10pm - 5:10pm)
Instructor: Dae Hyun Kim (daehyun@eecs.wsu.edu)

| Name: |  |
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| WSU ID: |  |

* Allowed: Textbooks, cheat sheets, class notes, notebooks, calculators, watches, electronic devices.
* Not allowed: Chat apps.


## Problem \#1 (Sequential Logic, 10 points)

The left one is a positive-edge-triggered explicit-pulsed D flip-flop (epDFF). The right one is a negative-edge-triggered epDFF.


Do the two FFs have the same hold-time constraint for $\mathrm{D}=0$ ?

Do the two FFs have the same hold-time constraint for $\mathrm{D}=1$ ?

## Problem \#2 (Domino Logic, 10 points)

The following shows a three-stage domino logic for $Y=N 1 \cdot N 2 \cdot N 3$ (the inputs to the NFET networks are not shown). The sizes of all the PFETs and the inverters are fixed (constants). All the given timing constraints are also fixed.


Now, we merge the PFETs into a single PFET as follows:


1) Will it work? If no, explain why. If yes, can you compare the size of the PFET in the second schematic and the sum of the sizes of the PFETs in the first schematic?

Now, let's merge the NFETs into a single NFET as follows:

2) Will it work? If no, explain why. If yes, can you compare the size of the clock NFET in the third schematic and the sum of the sizes of the clock NFETs in the first schematic?

## Problem \#3 (Sequential Logic, 10 points)

The following shows a schematic of a D-F/F. Estimate the hold time constraint of the F/F (for example, "one inverter delay + one transmission gate delay").


When the clock signal goes high, the transmission gate on the left side (TG1) is fully turned off after four inverter delays. Once it is turned off, even if D changes, nothing happens at the output node. Thus, the hold time constraint is "four inverter delay."

## Problem \#4 (Carry Select Adder, 10 points)

The following shows a schematic of a $2 k$-bit carry select adder designed using $k$-bit parallel adders. The delay of a $k$-bit adder is $\Delta_{F A} \cdot \log _{2} k$, the delay of a $k$-bit MUX is $\Delta_{M}$, and the delay of a two-input AND (or OR) gate is $\Delta_{M}$.


We are supposed to design an $N$-bit adder using carry select adders (\# groups: $\frac{N}{k}$ ). Find $k$ minimizing the delay of the $N$-bit adder (express the optimal $k$ as a function of $N, \Delta_{M}$, and $\Delta_{F A}$ ). Notice that the worst-case delay occurs at $C_{N}$ (the final carry out) or $S_{N-1: 0}$ (the final sum). Just a small math hint: $\log _{2} k=\frac{\ln k}{\ln 2}, \frac{d(\ln x)}{d x}=\frac{1}{x}$.

$$
\begin{gathered}
\tau=\Delta_{F A} \cdot \log _{2} k+\left(\frac{N}{k}-1\right) \cdot 2 \Delta_{M} \\
\frac{d \tau}{d k}=\frac{\Delta_{F A}}{\ln 2} \cdot \frac{1}{k}-\frac{2 N \Delta_{M}}{k^{2}}=0 \\
\therefore k=\frac{2 N \Delta_{M} \ln 2}{\Delta_{F A}}
\end{gathered}
$$

## Problem \#5 (Carry Select Adder, 10 points)

To radically improve the delay of a carry-select adder, we design an $N$-bit carry-select adder as follows:


We design the $k$-bit adder using a $k$-bit parallel adder where $k$ is $2 m^{i}$ ( $i$ is an integer greater than or equal to 0 ).

The following shows the delays of the components:

- $k$-bit adder: $\Delta_{F A} \cdot \log _{2} k=\Delta_{F A} \cdot \log _{2}\left(2 m^{i}\right)=\Delta_{F A} \cdot\left(1+i \cdot \log _{2} m\right)$
- $k$-bit MUX: $\Delta_{M}$
- $\Delta_{F A}>2 * \Delta_{M}$

Express the delay of the last carry out $C_{N}$ using $N, m, \Delta_{F A}$, and $\Delta_{M}$.
Delay of $C_{2}: \tau_{2}=\Delta_{F A}$
Delay of the $2 m$-bit adder: $d_{2 m}=\Delta_{F A} \cdot\left(1+\log _{2} m\right)$
Delay of $C_{2 m+2}: \tau_{2 m+2}=\operatorname{MAX}\left(\tau_{2}, d_{2 m}\right)+2 \Delta_{M}=\Delta_{F A} \cdot\left(1+\log _{2} m\right)+2 \Delta_{M}$
Delay of the $2 m^{2}$-bit adder: $d_{2 m^{\prime}}=\Delta_{F A} \cdot\left(1+2 \log _{2} m\right)$
Delay of $C_{2 m^{2}+2 m+2}: \tau_{2 m^{2}+2 m+2}=\operatorname{MAX}\left(\tau_{2 m+2}, d_{2 m^{\prime}}\right)+2 \Delta_{M}=\Delta_{F A} \cdot\left(1+2 \log _{2} m\right)+2 \Delta_{M}$
...
Delay of $C_{N}: \Delta_{F A} \cdot\left(1+x \cdot \log _{2} m\right)+2 \Delta_{M}$ where $x$ satisfies

$$
2+2 m+2 m^{2}+\cdots+2 m^{x}=N
$$

$$
\begin{gathered}
2+2 m+\cdots+2 m^{x}=\frac{2\left(m^{x+1}-1\right)}{m-1}=N \\
x=\frac{\ln \left(1+\frac{N(m-1)}{2}\right)}{\ln m}-1
\end{gathered}
$$

Thus, the delay of the last carry out is

$$
\Delta_{F A} \cdot\left(1+\left\{\frac{\ln \left(1+\frac{N(m-1)}{2}\right)}{\ln m}-1\right\} \cdot \log _{2} m\right)+2 \Delta_{M}
$$

## Problem \#6 (Carry Skip Adder, 20 points)

The following diagram shows a 16-bit carry-skip adder designed using 4-bit adders.


1) Show the details of the calculations in the carry skip adder for the following inputs (fill in the blanks).

$$
\begin{gathered}
A=0101010101010101 \\
B=1010101010101010 \\
C_{0}=1
\end{gathered}
$$

Step 1)
$[3: 0] g_{0}=0 . \quad g_{1}=0 . g_{2}=0 . g_{3}=0 . \quad p_{0}=1 . \quad p_{1}=1 . \quad p_{2}=1 . \quad p_{3}=1$.
[7:4] $g_{4}=0 . \quad g_{5}=0 . \quad g_{6}=0 . \quad g_{7}=0 . \quad p_{4}=1 . \quad p_{5}=1 . \quad p_{6}=1 . \quad p_{7}=1$.
$[11: 8] g_{8}=0 . \quad g_{9}=0 . \quad g_{10}=0 . \quad g_{11}=0 . \quad p_{8}=1 . \quad p_{9}=1 . \quad p_{10}=1 . \quad p_{11}=1$.
$[15: 12] g_{12}=0 . \quad g_{13}=0 . \quad g_{14}=0 . \quad g_{15}=0 . \quad p_{12}=1 . \quad p_{13}=1 . \quad p_{14}=1 . \quad p_{15}=1$.

Step 2)
$[3: 0] g_{1: 0}=0 . \quad p_{1: 0}=1 . \quad g_{2: 0}=0 . \quad p_{2: 0}=1 . \quad g_{3: 0}=0 . \quad p_{3: 0}=1$.
$[7: 4] g_{5: 4}=0 . \quad p_{5: 4}=1 . \quad g_{6: 4}=0 . \quad p_{6: 4}=1 . \quad g_{7: 4}=0 . \quad p_{7: 4}=1$.
$[11: 8] g_{9: 8}=0 . \quad p_{9: 8}=1 . \quad g_{10: 8}=0 . \quad p_{10: 8}=1 . \quad g_{11: 8}=0 . \quad p_{11: 8}=1$.
$[15: 12] g_{13: 12}=0 . \quad p_{13: 12}=1 . \quad g_{14: 12}=0 . \quad p_{14: 12}=1 . \quad g_{15: 12}=0 . \quad p_{15: 12}=1$.

Step 3)
[3:0] $c_{1}=1 . \quad c_{2}=1 . \quad c_{3}=1$.
$c_{4}=1$.

Step 4)
$[3: 0] s_{0}=0 . \quad s_{1}=0 . \quad s_{2}=0 . \quad s_{3}=0$.
$[7: 4] c_{5}=1 . \quad c_{6}=1 . \quad c_{7}=1$.
$c_{8}=1$.

Step 5)
$[7: 4] s_{4}=0 . \quad s_{5}=0 . \quad s_{6}=0 . \quad s_{7}=0$.
$[11: 8] c_{9}=1 . \quad c_{10}=1 . \quad c_{11}=1$.
$c_{12}=1$.

Step 6)
$[11: 8] s_{8}=0 . \quad s_{9}=0 . \quad s_{10}=0 . \quad s_{11}=0$.
[15:12] $c_{13}=1 . \quad c_{14}=1 . \quad c_{15}=1$.
$c_{16}=1$.

Step 7)
[15:12] $s_{12}=0 . \quad s_{13}=0 . \quad s_{14}=0 . \quad s_{15}=0$.
2) Repeat it for the following inputs.

$$
\begin{gathered}
A=0101010101010101 \\
B=1010101011101010 \\
C_{0}=1
\end{gathered}
$$

Step 1)
$[3: 0] g_{0}=0 . \quad g_{1}=0 . \quad g_{2}=0 . \quad g_{3}=0 . \quad p_{0}=1 . \quad p_{1}=1 . \quad p_{2}=1 . \quad p_{3}=1$.
[7:4] $g_{4}=0 . \quad g_{5}=0 . \quad g_{6}=1 . \quad g_{7}=0 . \quad p_{4}=1 . \quad p_{5}=1 . \quad p_{6}=0 . \quad p_{7}=1$.
[11:8] $g_{8}=0 . \quad g_{9}=0 . \quad g_{10}=0 . \quad g_{11}=0 . \quad p_{8}=1 . \quad p_{9}=1 . \quad p_{10}=1 . \quad p_{11}=1$.
[15:12] $g_{12}=0 . \quad g_{13}=0 . g_{14}=0 . \quad g_{15}=0 . \quad p_{12}=1 . \quad p_{13}=1 . \quad p_{14}=1 . \quad p_{15}=1$.

Step 2)
$[3: 0] g_{1: 0}=0 . \quad p_{1: 0}=1 . \quad g_{2: 0}=0 . \quad p_{2: 0}=1 . \quad g_{3: 0}=0 . \quad p_{3: 0}=1$.
$[7: 4] g_{5: 4}=0 . \quad p_{5: 4}=1 . \quad g_{6: 4}=1 . \quad p_{6: 4}=0 . \quad g_{7: 4}=1 . \quad p_{7: 4}=0$.
$[11: 8] g_{9: 8}=0 . \quad p_{9: 8}=1 . \quad g_{10: 8}=0 . \quad p_{10: 8}=1 . \quad g_{11: 8}=0 . \quad p_{11: 8}=1$.
[15:12] $g_{13: 12}=0 . \quad p_{13: 12}=1 . \quad g_{14: 12}=0 . \quad p_{14: 12}=1 . \quad g_{15: 12}=0 . \quad p_{15: 12}=1$.

Step 3)
[3:0] $c_{1}=1 . \quad c_{2}=1 . \quad c_{3}=1$.
$c_{4}=1$.

Step 4)
[3:0] $s_{0}=0 . \quad s_{1}=0 . \quad s_{2}=0 . \quad s_{3}=0$.
$[7: 4] c_{5}=1 . \quad c_{6}=1 . \quad c_{7}=1$.
$c_{8}=1$.

Step 5)
$[7: 4] s_{4}=0 . s_{5}=0 . \quad s_{6}=1 . \quad s_{7}=0$.
[11:8] $c_{9}=1 . \quad c_{10}=1 . \quad c_{11}=1$.
$c_{12}=1$.

Step 6)
$[11: 8] s_{8}=0 . \quad s_{9}=0 . \quad s_{10}=0 . \quad s_{11}=0$.
[15:12] $c_{13}=1 . \quad c_{14}=1 . \quad c_{15}=1$.
$c_{16}=1$.

Step 7)
[15:12] $s_{12}=0 . s_{13}=0 . s_{14}=0 . s_{15}=0$.

## Problem \#7 (Prefix Adder, 10 points)

Use the following delay values:

- AND, OR, XOR: $\Delta$
- Two-level (sum-of-product) logic: $2 \Delta$
- $g_{i}=a_{i} \cdot b_{i}, p_{i}=a_{i} \oplus b_{i}$

We are designing a 1024-bit Kogge-Stone adder.
Represent $s_{885}$ hierarchically using group-generated and group-propagated carries ( $g_{i: k}, p_{i: k}$ ) and $c_{0}$ (primary carry-in), then compute the delay to compute $s_{885}$ assuming all the primary input signals are available at time 0 (10 points).

$$
\begin{gathered}
s_{885}=p_{885} \oplus c_{885} \\
c_{885}=g_{884: 0}+p_{884: 0} \cdot c_{0} \\
g_{884: 0}=g_{884: 373}+p_{884: 373} \cdot g_{372: 0}\left(p_{884: 0}=p_{884: 373} \cdot p_{372: 0}\right) \\
g_{884: 373}=g_{884: 629}+p_{884: 629} \cdot g_{628: 373} \\
g_{884: 629}=g_{884: 757}+p_{884: 757} \cdot g_{756: 629} \\
g_{884: 757}=g_{884: 821}+p_{884: 821} \cdot g_{820: 757} \\
g_{884: 821}=g_{884: 853}+p_{884: 853} \cdot g_{852: 821} \\
g_{884: 853}=g_{884: 869}+p_{884: 869} \cdot g_{868: 853} \\
g_{884: 869}=g_{884: 877}+p_{884: 877} \cdot g_{876: 869} \\
g_{884: 877}=g_{884: 881}+p_{884: 881} \cdot g_{880: 877} \\
g_{884: 881}=g_{884: 883}+p_{884: 883} \cdot g_{882: 881} \\
g_{884: 883}=g_{884}+p_{884} \cdot g_{883}
\end{gathered}
$$

Delay $=\Delta+2 \Delta+2 \Delta+2 \Delta+2 \Delta+2 \Delta+2 \Delta+2 \Delta+2 \Delta+2 \Delta+2 \Delta+2 \Delta+\Delta=24 \Delta$

## Problem \#8 (Prefix Adder, 10 points)

Use the following delay values:

- AND, OR, XOR: $\Delta$
- Two-level (sum-of-product) logic: $2 \Delta$
- $g_{i}=a_{i} \cdot b_{i}, p_{i}=a_{i} \oplus b_{i}$

We are designing a 1024-bit adder, which is similar to the Kogge-Stone adder. However, we will design the adder as follows.

- Step 0: Compute $g_{i}$ and $p_{i}$.
- Step 1: Instead of generating $g_{i: i-1}, p_{i: i-1}$ for each $i$ by merging $g_{i}, p_{i}$ and $g_{i-1}, p_{i-1}$, generate $g_{i: i-3}, p_{i: i-3}$ for each $i$ (except $i=0,1,2$. For $\mathrm{i}=1$, merge $g_{1}, p_{1}, g_{0}, p_{0}$. For $\mathrm{i}=2$, merge $g_{2}, p_{2}, \ldots, g_{0}, p_{0}$ ) by merging $g_{i}, p_{i}, g_{i-1}, p_{i-1}, g_{i-2}, p_{i-2}, g_{i-3}, p_{i-3}$.
- Step 2: Generate $g_{i: i-15}, p_{i: i-15}$ for each $i$ by merging
$g_{i: i-3}, p_{i: i-3}, g_{i-4: i-7}, p_{i-4: i-7}, g_{i-8: i-11}, p_{i-8: i-11}, g_{i-12: i-15}, p_{i-12: i-15}$. Notice that this cannot be applied to $i=0, \ldots, 14$. However, you can generate $g_{i: 0}, p_{i: 0}$ for them properly.
- $\quad$ Step 3: Generate $g_{i: i-63}, p_{i: i-63}$ for each $i$.
- Repeat.

Represent $s_{885}$ hierarchically using group-generated and group-propagated carries ( $g_{i: k}, p_{i: k}$ ) and $c_{0}$ (primary carry-in), then compute the delay to compute $s_{885}$ assuming all the primary input signals are available at time 0 ( 10 points).

$$
\begin{gathered}
s_{885}=p_{885} \oplus c_{885} \\
c_{885}=g_{884: 0}+p_{884: 0} \cdot c_{0} \\
g_{884: 0}=g_{884: 629}+p_{884: 629} \cdot g_{628: 373}+p_{884: 629} \cdot p_{628: 373} \cdot g_{372: 117}+p_{884: 629} \cdot p_{628: 373} \\
\cdot p_{372: 117} \cdot g_{116: 0} \\
\left(p_{884: 0}=p_{884: 629} \cdot p_{628: 373} \cdot p_{372: 117} \cdot p_{116: 0}\right) \\
g_{884: 629}=g_{884: 821}+p_{884: 821} \cdot g_{820: 757}+p_{884: 821} \cdot p_{820: 757} \cdot g_{756: 693}+p_{884: 821} \cdot p_{820: 757} \\
\cdot p_{756: 693} \cdot g_{692: 629} \\
g_{884: 821}=g_{884: 869}+p_{884: 869} \cdot g_{868: 853}+p_{884: 869} \cdot p_{868: 853} \cdot g_{852: 837}+p_{884: 869} \cdot p_{868: 853} \\
\cdot p_{852: 837} \cdot g_{836: 821} \\
g_{884: 869}=g_{884: 881}+p_{884: 881} \cdot g_{880: 877}+p_{884: 881} \cdot p_{880: 877} \cdot g_{876: 873}+p_{884: 881} \cdot p_{880: 877} \\
\cdot p_{876: 873} \cdot g_{872: 869} \\
g_{884: 881}=g_{884}+p_{884} \cdot g_{883}+p_{884} \cdot p_{883} \cdot g_{882}+p_{884} \cdot p_{883} \cdot p_{882} \cdot g_{881}
\end{gathered}
$$

Delay $=\Delta+2 \Delta+2 \Delta+2 \Delta+2 \Delta+2 \Delta+2 \Delta+\Delta=14 \Delta$

## Problem \#9 (Carry Look-Ahead Adder, 40 points)

The max. fanout is 4 . Use the following delay values:

- AND, OR, XOR: $\Delta$
- Two-level (sum-of-product) logic: $2 \Delta$
- $g_{i}=a_{i} \cdot b_{i}, p_{i}=a_{i} \oplus b_{i}$

We are designing a 2048-bit carry look-ahead adder.

1) Represent $s_{885}$ hierarchically using group-generated and group-propagated carries ( $g_{i: k}, p_{i: k}$ ) and $c_{0}$ (primary carry-in), then compute the delay to compute $s_{885}$ assuming all the primary input signals are available at time 0 (10 points).

$$
\begin{gathered}
s_{885}=p_{885} \oplus c_{885} \\
c_{885}=g_{884}+p_{884} \cdot c_{884} \\
c_{884}=g_{883: 880}+p_{883: 880} \cdot c_{880} \\
c_{880}=g_{879: 864}+p_{879: 864} \cdot g_{863: 848}+p_{879: 864} \cdot p_{863: 848} \cdot g_{847: 832}+p_{879: 864} \cdot p_{863: 848} \\
\cdot p_{847: 832} \cdot c_{832} \\
c_{832}=g_{831: 768}+p_{831: 768} \cdot c_{768} \\
c_{768}=g_{767: 512}+p_{767: 512} \cdot g_{511: 256}+p_{767: 512} \cdot p_{511: 256} \cdot g_{255: 0}+p_{767: 512} \cdot p_{511: 256} \cdot p_{255: 0} \\
c_{0} \\
g_{255: 0}=g_{255: 192}+p_{255: 192} \cdot g_{191: 128}+p_{255: 192} \cdot p_{191: 128} \cdot g_{127: 64}+p_{255: 192} \cdot p_{191: 128} \cdot p_{127: 64} \\
g_{63: 0}=g_{63: 48}+p_{63: 48} \cdot g_{47: 32}+p_{63: 48} \cdot p_{47: 32} \cdot g_{31: 16}+p_{63: 48} \cdot p_{47: 32} \cdot p_{31: 16} \cdot g_{15: 0} \\
g_{15: 0}=g_{15: 12}+p_{15: 12} \cdot g_{11: 8}+p_{15: 12} \cdot p_{11: 8} \cdot g_{7: 4}+p_{15: 12} \cdot p_{11: 8} \cdot p_{7: 4} \cdot g_{3: 0} \\
g_{3: 0}=g_{3}+p_{3} \cdot g_{2}+p_{3} \cdot p_{2} \cdot g_{1}+p_{3} \cdot p_{2} \cdot p_{1} \cdot g_{0} \\
\text { Delay }=\Delta+2 \Delta+2 \Delta+2 \Delta+2 \Delta+2 \Delta+2 \Delta+2 \Delta+2 \Delta+2 \Delta+\Delta=20 \Delta
\end{gathered}
$$

2) Represent $s_{2019}$ hierarchically using group-generated and group-propagated carries ( $g_{i: k}, p_{i: k}$ ) and $c_{0}$ (primary carry-in), then compute the delay to compute $s_{2019}$ assuming all the primary input signals are available at time 0 (10 points).

$$
\begin{gathered}
s_{2019}=p_{2019} \oplus c_{2019} \\
c_{2019}=g_{2018}+p_{2018} \cdot g_{2017}+p_{2018} \cdot p_{2017} \cdot g_{2016}+p_{2018} \cdot p_{2017} \cdot p_{2016} \cdot c_{2016} \\
c_{2016}=g_{2015: 2000}+p_{2015: 2000} \cdot g_{1999: 1984}+p_{2015: 2000} \cdot g_{1999: 1984} \cdot c_{1984} \\
c_{1984}=g_{1983: 1920}+p_{1983: 1920} \cdot g_{1919: 1856}+p_{1983: 1920} \cdot p_{1919: 1856} \cdot g_{1855: 1792}+p_{1983: 1920} \\
\cdot p_{1919: 1856} \cdot p_{1855: 1792} \cdot c_{1792} \\
c_{1792}=g_{1791: 1536}+p_{1791: 1536} \cdot g_{1535: 1280}+p_{1791: 1536} \cdot p_{1535: 1280} \cdot g_{1279: 1024}+p_{1791: 1536} \\
\cdot p_{1535: 1280} \cdot p_{1279: 1024} \cdot c_{1024} \\
c_{1024}=g_{1023: 0}+p_{1023: 0} \cdot c_{0} \\
g_{1023: 0}=g_{1023: 768}+p_{1023: 768} \cdot g_{767: 512}+p_{1023: 768} \cdot p_{767: 512} \cdot g_{511: 256}+p_{1023: 768} \cdot p_{767: 512} \\
\cdot p_{511: 256} \cdot g_{255: 0} \\
g_{255: 0}=g_{255: 192}+p_{255: 192} \cdot g_{191: 128}+p_{255: 192} \cdot p_{191: 128} \cdot g_{127: 64}+p_{255: 192} \cdot p_{191: 128} \cdot p_{127: 64} \\
\cdot g_{63: 0} \\
g_{63: 0}=g_{63: 48}+p_{63: 48} \cdot g_{47: 32}+p_{63: 48} \cdot p_{47: 32} \cdot g_{31: 16}+p_{63: 48} \cdot p_{47: 32} \cdot p_{31: 16} \cdot g_{15: 0} \\
g_{15: 0}=g_{15: 12}+p_{15: 12} \cdot g_{11: 8}+p_{15: 12} \cdot p_{11: 8} \cdot g_{7: 4}+p_{15: 12} \cdot p_{11: 8} \cdot p_{7: 4} \cdot g_{3: 0} \\
g_{3: 0}=g_{3}+p_{3} \cdot g_{2}+p_{3} \cdot p_{2} \cdot g_{1}+p_{3} \cdot p_{2} \cdot p_{1} \cdot g_{0} \\
\text { Delay }=\Delta+2 \Delta+2 \Delta+2 \Delta+2 \Delta+2 \Delta+2 \Delta+2 \Delta+2 \Delta+2 \Delta+2 \Delta+\Delta=22 \Delta
\end{gathered}
$$

3) Show details of the calculations in the 16-bit carry-lookahead adder for the following inputs (show $g_{i}, p_{i}$, group generation/propagation bits, carry signals, etc.) Draw some block diagrams too for the carry-lookahead units and show the values of the signals.

$$
\begin{gathered}
A=0101010101010101 \\
B=1010101010101010 \\
C_{0}=1
\end{gathered}
$$

You can show the details like the one in Problem 6.
Step 1)
$[3: 0] g_{0}, g_{1}, g_{2}, g_{3}=0 . p_{0}, p_{1}, p_{2}, p_{3}=1$.
$[7: 4] g_{4}, g_{5}, g_{6}, g_{7}=0 . \quad p_{4}, p_{5}, p_{6}, p_{7}=1$.
$[11: 8] g_{8}, g_{9}, g_{10}, g_{11}=0 . \quad p_{8}, p_{9}, p_{10}, p_{11}=1$.
$[15: 12] g_{12}, g_{13}, g_{14}, g_{15}=0 . \quad p_{12}, p_{13}, p_{14}, p_{15}=1$.

Step 2)
$[3: 0] g_{3: 0}=0 . \quad p_{3: 0}=1 . \quad c_{1}=g_{0}+p_{0} c_{0}=1 . \quad c_{2}=g_{1}+p_{1} g_{1}+p_{1} p_{0} c_{0}=1 . \quad c_{3}=g_{2}+$ $p_{2} g_{1}+p_{2} p_{1} g_{0}+p_{2} p_{1} p_{0} c_{0}=1$.
$[7: 4] g_{7: 4}=0 . \quad p_{7: 4}=1$.
$[11: 8] g_{11: 8}=0 . \quad p_{11: 8}=1$.
$[15: 12] g_{15: 12}=0 . \quad p_{15: 12}=1$.

Step 3)
$[3: 0] s_{0}=p_{0} \oplus c_{0}=0 . \quad s_{1}=0 . \quad s_{2}=0 . \quad s_{3}=0$.
$c_{4}=g_{3: 0}+p_{3: 0} c_{0}=1 . \quad c_{8}=g_{7: 4}+p_{7: 4} g_{3: 0}+p_{7: 4} p_{3: 0} c_{0}=1 . \quad c_{12}=g_{11: 8}+p_{11: 8} g_{7: 4}+$ $p_{11: 8} p_{7: 4} g_{3: 0}+p_{11: 8} p_{7: 4} p_{3: 0} c_{0}=1$.
$g_{15: 0}=0 . \quad p_{15: 0}=1$.

Step 4)
$c_{16}=g_{15: 0}+p_{15: 0} c_{0}=1$.
$[7: 4] c_{5}=1 . \quad c_{6}=1 . \quad c_{7}=1$.
$[11: 8] \quad c_{9}=1 . \quad c_{10}=1 . \quad c_{11}=1$.
[15:12] $c_{13}=1 . \quad c_{14}=1 . \quad c_{15}=1$.

Step 5)
$[7: 4] s_{4}=0 . \quad s_{5}=0 . \quad s_{6}=0 . \quad s_{7}=0$.
$[11: 8] s_{8}=0 . \quad s_{9}=0 . \quad s_{10}=0 . \quad s_{11}=0$.
[15:12] $s_{12}=0 . \quad s_{13}=0 . \quad s_{14}=0 . \quad s_{15}=0$.
4) Repeat it for the following inputs.

$$
\begin{gathered}
A=0101010101010101 \\
B=1010101011101010 \\
C_{0}=1
\end{gathered}
$$

Step 1)
$[3: 0] g_{0}, g_{1}, g_{2}, g_{3}=0 . p_{0}, p_{1}, p_{2}, p_{3}=1$.
$[7: 4] g_{4}, g_{5}, g_{7}=0 . \quad g_{6}=1 . \quad p_{4}, p_{5}, p_{7}=1 . \quad p_{6}=0$.
$[11: 8] g_{8}, g_{9}, g_{10}, g_{11}=0 . \quad p_{8}, p_{9}, p_{10}, p_{11}=1$.
$[15: 12] g_{12}, g_{13}, g_{14}, g_{15}=0 . \quad p_{12}, p_{13}, p_{14}, p_{15}=1$.

Step 2)
$[3: 0] g_{3: 0}=0 . \quad p_{3: 0}=1 . \quad c_{1}=g_{0}+p_{0} c_{0}=1 . \quad c_{2}=g_{1}+p_{1} g_{1}+p_{1} p_{0} c_{0}=1 . \quad c_{3}=g_{2}+$ $p_{2} g_{1}+p_{2} p_{1} g_{0}+p_{2} p_{1} p_{0} c_{0}=1$.
$[7: 4] g_{7: 4}=1 . \quad p_{7: 4}=0$.
$[11: 8] g_{11: 8}=0 . \quad p_{11: 8}=1$.
$[15: 12] g_{15: 12}=0 . \quad p_{15: 12}=1$.

Step 3)
$[3: 0] s_{0}=p_{0} \oplus c_{0}=0 . \quad s_{1}=0 . \quad s_{2}=0 . \quad s_{3}=0$.
$c_{4}=g_{3: 0}+p_{3: 0} c_{0}=1 . \quad c_{8}=g_{7: 4}+p_{7: 4} g_{3: 0}+p_{7: 4} p_{3: 0} c_{0}=1 . \quad c_{12}=g_{11: 8}+p_{11: 8} g_{7: 4}+$ $p_{11: 8} p_{7: 4} g_{3: 0}+p_{11: 8} p_{7: 4} p_{3: 0} c_{0}=1$.
$g_{15: 0}=1 . \quad p_{15: 0}=0$.

Step 4)
$c_{16}=g_{15: 0}+p_{15: 0} c_{0}=1$.
$[7: 4] c_{5}=1 . \quad c_{6}=1 . \quad c_{7}=1$.
$[11: 8] c_{9}=1 . \quad c_{10}=1 . \quad c_{11}=1$.
[15:12] $c_{13}=1 . \quad c_{14}=1 . \quad c_{15}=1$.

Step 5)
$[7: 4] s_{4}=0 . \quad s_{5}=0 . \quad s_{6}=1 . \quad s_{7}=0$.
$[11: 8] s_{8}=0 . \quad s_{9}=0 . \quad s_{10}=0 . \quad s_{11}=0$.
[15:12] $s_{12}=0 . \quad s_{13}=0 . \quad s_{14}=0 . \quad s_{15}=0$.

