EE466

VLSI System Design

Midterm Exam

Oct. 24, 2018. (4:15pm – 5:30pm)

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Name:

WSU ID:

Problem	Points	
1	10	
2	10	
3	10	
4	10	
5	10	
6	10	
7	10	
8	10	
Total	80	

* Allowed: Textbooks, cheat sheets, class notes, notebooks, calculators, watches

* Not allowed: Electronic devices (smart phones, tablet PCs, laptops, etc.) except calculators and watches

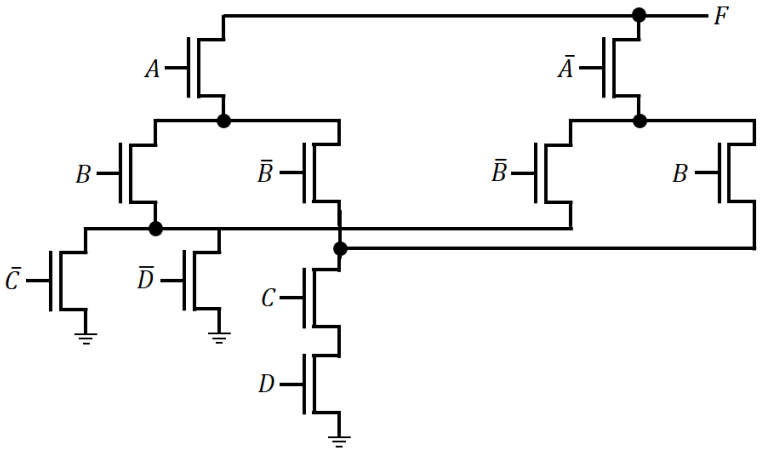
Problem #1 (Static CMOS Gates, 10 points).

Draw a transistor-level schematic for the NFET network of the following Boolean function (Available input: $A, B, C, D, \bar{A}, \bar{B}, \bar{C}, \bar{D}$). Use the static CMOS gate design. Minimize the # TRs.

TRs≤12: 10 points. 13≤# TRs≤14: 8 points. 15≤# TRs≤16: 5 points.

$$F = \overline{A \oplus (\overline{B \oplus (CD)})}$$

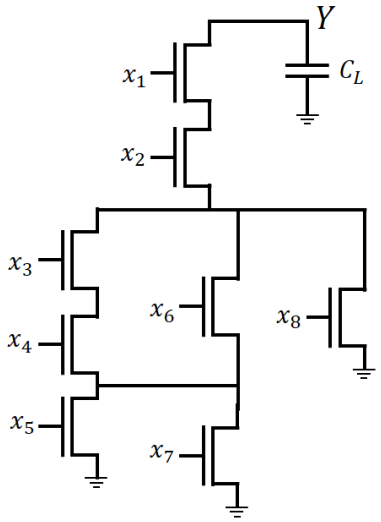
$$\bar{F} = A \oplus \left(\overline{B \oplus (CD)}\right) = A \oplus (\overline{B \oplus E}) = A(B \oplus E) + \bar{A} \cdot \overline{B \oplus E} = A \cdot (B\bar{E} + \bar{B}E) + \bar{A} \cdot (BE + \bar{B}\bar{E})$$
$$= A \cdot (B(\bar{C} + \bar{D}) + \bar{B}CD) + \bar{A} \cdot \left(BCD + \bar{B}(\bar{C} + \bar{D})\right)$$
$$= (AB + \bar{A}\bar{B})(\bar{C} + \bar{D}) + (A\bar{B} + \bar{A}B)CD$$



Problem #2 (Transistor Sizing, 10 points).

Size the transistors in the following pull-down network of a static CMOS gate. R_n is the resistance of a 1X NMOS transistor. C_L is the load cap. Ignore all the parasitic capacitances. Target timing constraint: $\tau = R_n \cdot C_L$. Try to minimize the total area.

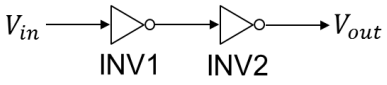
Area≤36X: 10 points. 36X<Area≤38X: 7 points. 38X<Area: 4 points.

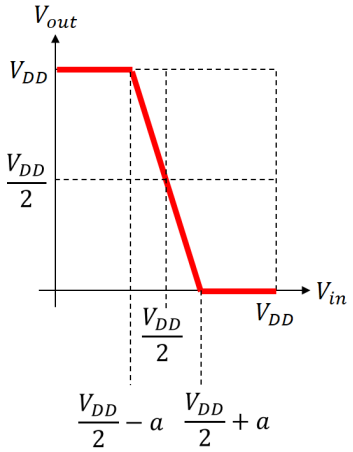


The longest path: x1-x2-x3-x4-(x5 or x7). All of them become 5X.

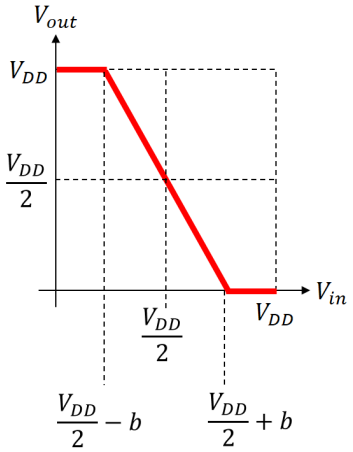
x_1: 5X
x_2: 5X
x_3: 5X
x_4: 5X
x_5: 5X
x_6: 2.5X
x_7: 5X
x_8: 5/3X

Problem #3 (DC Analysis, 10 points).





Char 1



Char 2

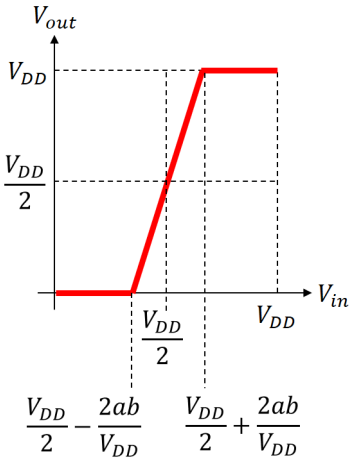
The gate-level schematic shows a buffer composed of two inverters.

Buffer 1: Char 1 for INV1 and Char 2 for INV2

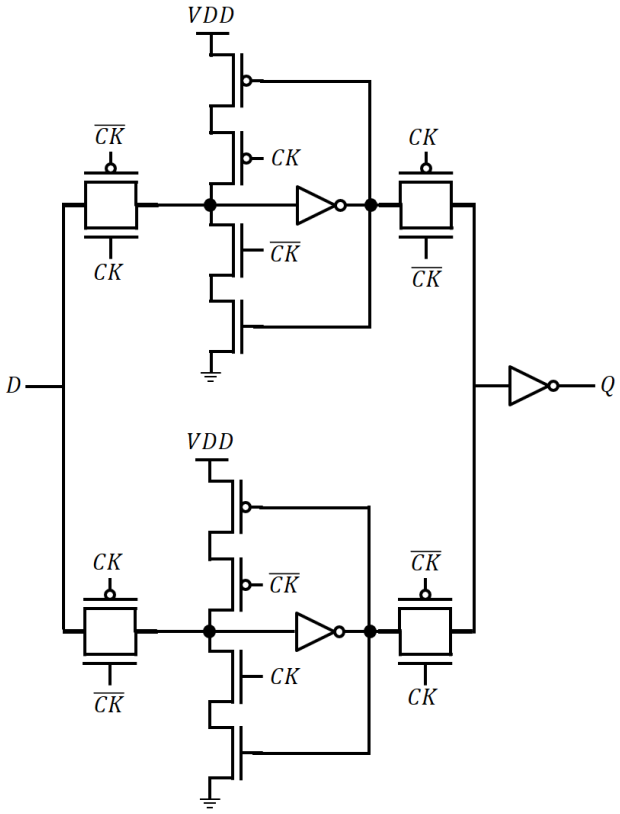
Buffer 2: Char 2 for INV1 and Char1 for INV2

Prove that the two buffers have the same DC characteristics.

Both of them have the same DC curve as follows:



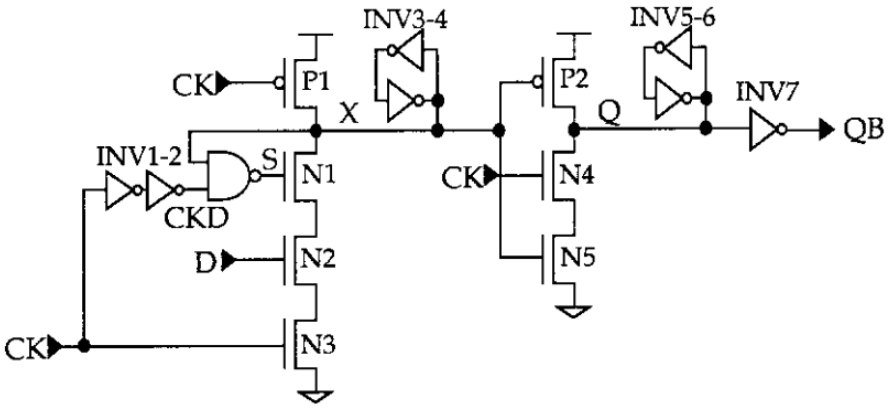
Problem #4 (Logic Analysis, 10 points).



Describe the function of the circuit shown above.

Dual-edge-triggered D-FF.

Problem #5 (Sequential Logic, 10 points).



The circuit shown above is a positive-edge-triggered D FF. Let T_X be the sum of the delays of the two inverters and the NAND gate.

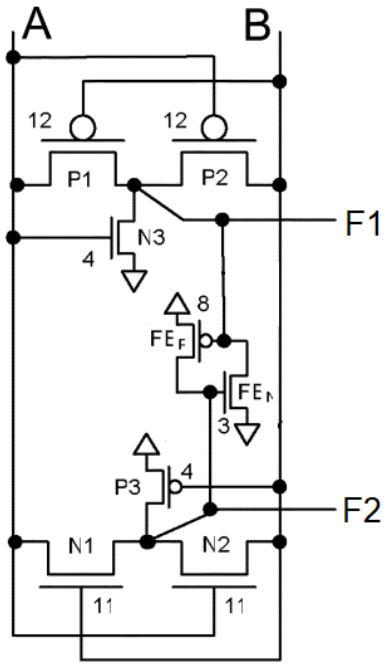
(1) Estimate the hold time of the FF for input D=0.

Suppose D=0. When CK goes high, N1 will be turned off after some delay. If D changes (i.e., becomes 1) before N1 is turned off, X will be discharged and Q will become 1. Thus, D should not change before N1 is turned off. Thus, the hold time for D=0 is T_X.

(2) Estimate the hold time for input D=1.

Suppose D=1. When CK goes high, X will be discharged. Once it is fully discharged, even if D becomes 0, there is no problem. Thus, the hold time for D=1 is T_d, which is the time to discharge node X.

Problem #6 (Logic Analysis, 10 points).



The above circuit has two inputs (A, B) and two outputs (F1 and F2).

(1) Express F1 as a Boolean function of A and B.

$$F1 = A \oplus B$$

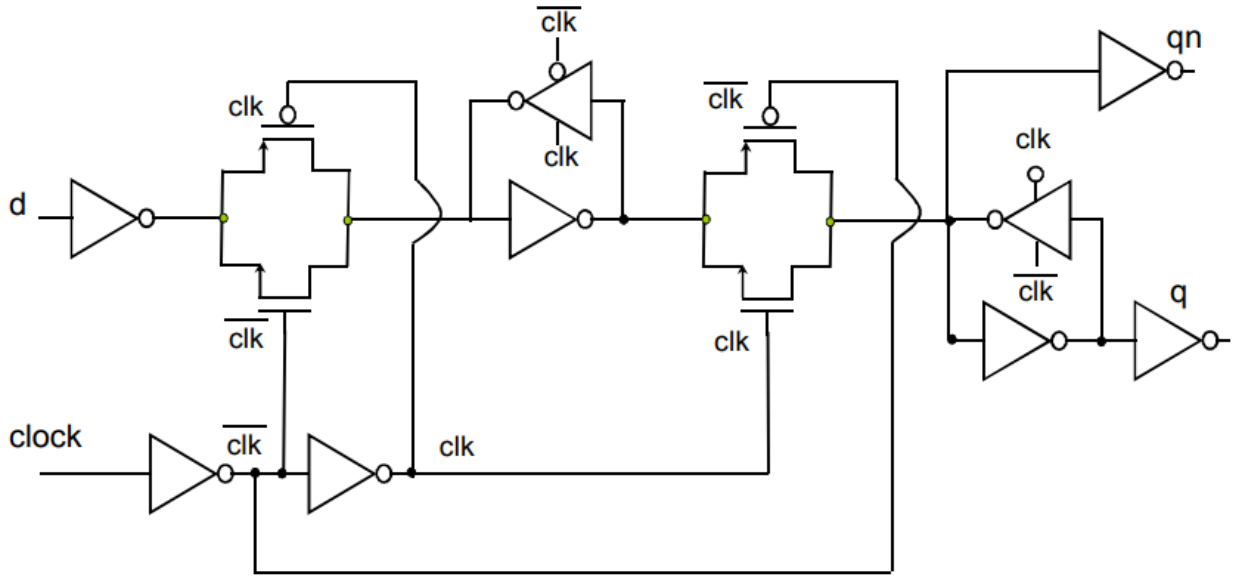
(2) Express F2 as a Boolean function of A and B.

$$F1 = \overline{A \oplus B}$$

(3) Does it have any static power consumption problem? Explain why (or why not).

When A=1, B=0, N3 is ON, but P1 is ON and A is connected to F1, so there is static power consumption. Same for A=0, B=1.

Problem #7 (Sequential Logic, 10 points).



The circuit shown above is a positive-edge-triggered D FF. Notice that all the inverters and transmission gates have finite delays.

(1) Estimate the hold time of the FF for input D=0.

The first TG will be turned off after two inverter delays. If D switches from 1 to 0, the output of the inverter connected to D will be 1 after one inverter delay. Thus, as long as D holds 0 for one inverter delay (+ delta), it is safe.

(2) Estimate the hold time for input D=1.

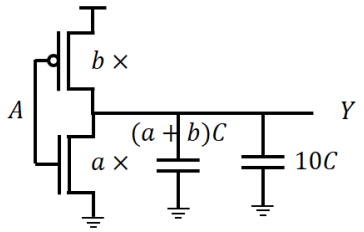
For the same reason, the hold time is one inverter delay + delta for D=1.

(3) Estimate the signal delay (from a clock rising edge at the clock input to Q).

When CK goes high, the second TG is closed after two inverter delays. Then, Q changes after a TG delay + two inverter delays.

Problem #8 (Power Consumption, 10 points).

The following figure shows an inverter with a parasitic cap and a load cap (10C). The parasitic cap is proportional to the sizes of the transistors connected to the cap. The PFET is upsized to bX and the NFET is upsized to aX. $\frac{\mu_n}{\mu_p} = 2$. The rising delay should be $\leq 20R_nC$ where R_n is the resistance of a 1X NFET. The falling delay should be $\leq 10R_nC$. Both a and b are integers.



Can you find a and b minimizing the power consumption and satisfying the given timing constraints? Notice that there are only a few combinations of (a, b) you need to calculate to answer this problem.

The rise delay is $t_r = \frac{R_p}{b} \cdot (a + b + 10)C$ and the fall delay is $t_f = \frac{R_n}{a} \cdot (a + b + 10)C$. The power consumption is $f(a + b + 10)C{V_{DD}}^2$, so minimizing the power is minimizing $a + b$.

$$t_r = \frac{2R_n}{b} \cdot (a + b + 10)C \leq 20R_nC, \text{ so } a + b + 10 \leq 10b, \text{ so } a + 10 \leq 9b.$$

$$t_f = \frac{R_n}{a} \cdot (a + b + 10)C \leq 10R_nC, \text{ so } a + b + 10 \leq 10a, \text{ so } b + 10 \leq 9a.$$

$$\frac{a+10}{9} \leq b \leq 9a - 10.$$

If a=1, b is negative.

If a=2, $1.XX \leq b \leq 8$, so b is 2 (to minimize a+b). In this case, a+b=4.

If a=3, b=2. If a>=4, a+b>=5.

Thus, $a = 2X, b = 2X$.