EE466

VLSI System Design

Midterm Exam

Dec. 14, 2020. (4pm – 6pm)

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Name:

WSU ID:

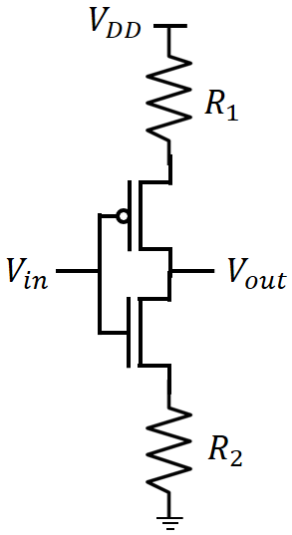
Problem	Points	
1	10	
2	10	
3	20	
4	10	
5	15	
6	10	
7	25	
8	25	
9	20	
Total	145	

* Allowed: Textbooks, cheat sheets, class notes, notebooks, calculators, watches

* Not allowed: Electronic devices (smart phones, tablet PCs, laptops, etc.) except calculators and watches

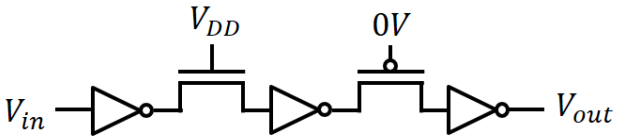
Problem #1 (DC Analysis, 10 points)

Draw a DC curve (V_{in} vs. V_{out}) for the following logic circuit. You should also show some important data points on the curve.



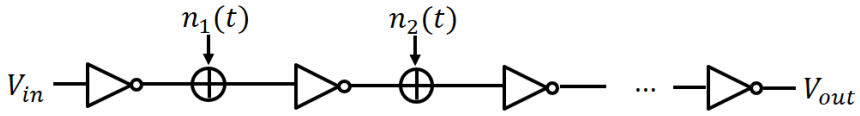
Problem #2 (DC Analysis, 10 points)

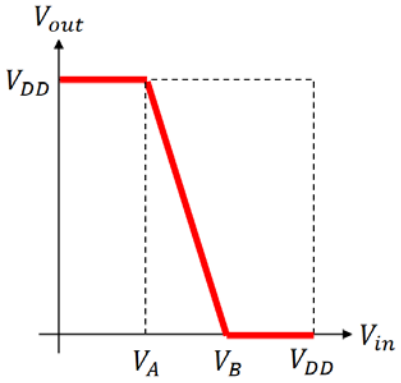
Draw a DC curve (V_{in} vs. V_{out}) for the following logic circuit. Assume $V_{th,n} = |V_{th,p}|$ for all the NFETs and PFETs. Just a rough sketch will be accepted.



Problem #3 (Noise, 20 points)

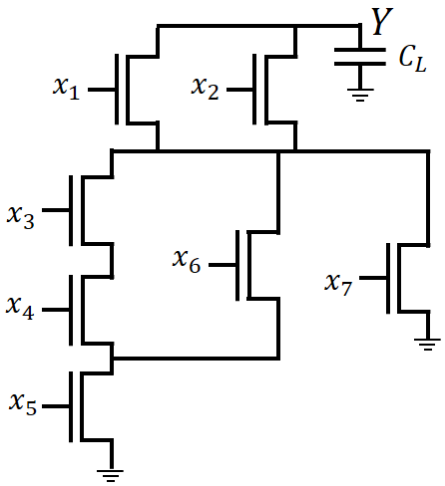
The following shows a chain of inverters. $n_i(t)$ is a noise source and added to the signal as shown below. The range of $n_i(t)$ is $[-\frac{V_{DD}}{8}, \frac{V_{DD}}{4}]$. All the inverters have the same DC characteristics shown below. V_{in} is 0V for logic 0 and V_{DD} for logic 1. Assume that $0 < V_A \leq \frac{V_{DD}}{4} \leq V_B \leq \frac{7V_{DD}}{8}$. Find equations and/or inequalities that V_A and V_B should satisfy to avoid signal inversion.





Problem #4 (Transistor Sizing, 10 points)

Size the transistors in the following NFET network of a static CMOS gate. R_n is the resistance of a 1X NFET. C_L is the load cap. Ignore all the parasitic capacitances. Target timing constraint: $\tau \leq R_n \cdot C_L$. Try to minimize the total area.



Area≤ 24X: 10 points. 24X<Area≤ 26X: 7 points. 26X<Area: 4 points.

x_1:

x_2:

x_3:

x_4:

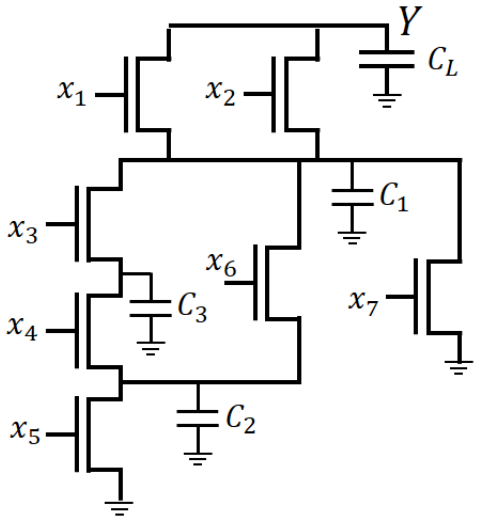
x_5:

x_6:

x_7:

Problem #5 (Switching Characteristics, 15 points)

The following shows the NFET network of a logic gate designed by the static CMOS design methodology. It also shows a load capacitor C_L and three parasitic capacitors C_1, C_2, and C_3. The resistance of transistor x_k is R_k. Assume that all the capacitors are fully charged before we discharge them.



(1) Express the fall delay as a function of R_k and C_m ($k = 1, \ldots, 7$, $m = 1,2,3, L$) for $(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$=(1,0,1,1,1,0,0).

(2) Express the fall delay as a function of R_k and C_m ($k = 1, \ldots, 7$, $m = 1,2,3, L$) for $(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$=(1,1,0,0,1,1,0).

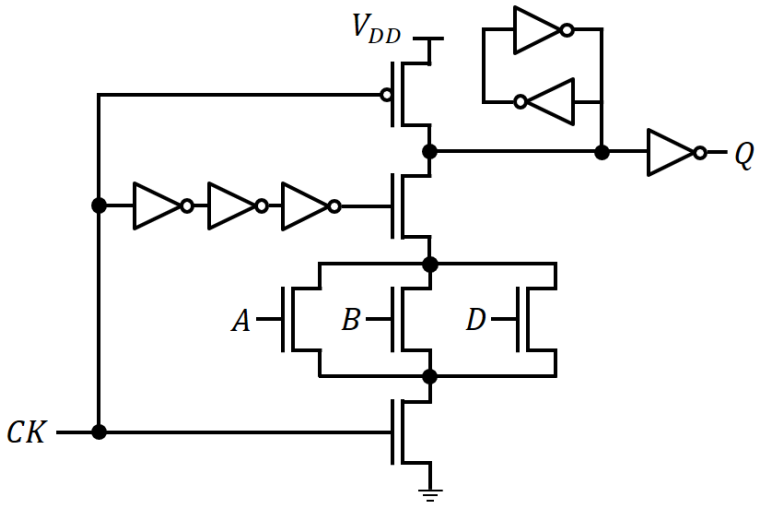
(3) Express the fall delay as a function of R_k and C_m ($k = 1, \ldots, 7$, $m = 1,2,3, L$) for $(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$=(0,1,0,0,0,0,1).

Problem #6 (Memory, 10 points)

We want to design a register file having 16 64-bit registers and supporting four simultaneous accesses (i.e., we can access four different registers at the same time). Draw a 12-transistor SRAM cell supporting the four simultaneous accesses. The Word-line signals are W_0, W_1, W_2, W_3. The four pairs of Bit-line signals are $(B_0, \overline{B_0}), (B_1, \overline{B_1}), (B_2, \overline{B_2}), (B_3, \overline{B_3})$. You should show the Word-line and Bit-line signals too in your figure.

Problem #7 (Flip-Flop, 25 points).

The following schematic shows a positive-edge-triggered D flip-flop. CK is the clock input, Q is the output, and A, B, D are signal inputs. Answer the following questions.



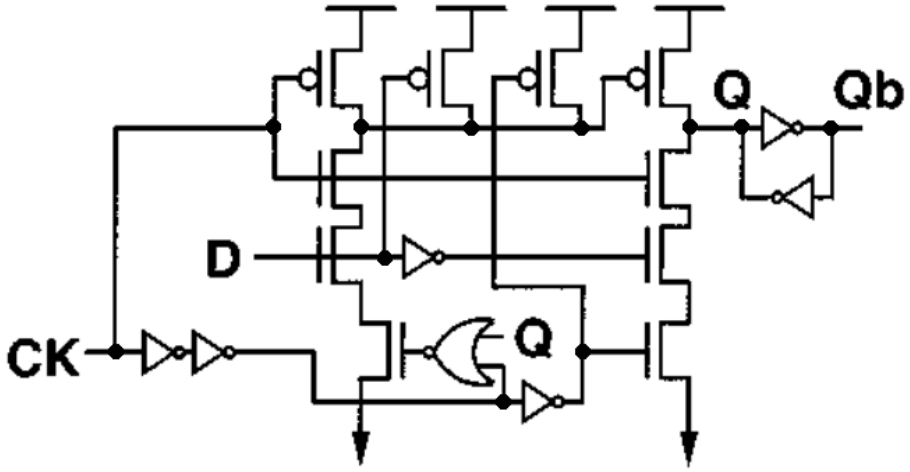
(1) Express the output Q as a function of the input signals A, B, and D.

(2) Explain how you can estimate the setup time of the FF.

(3) Explain how you can estimate the hold time of the FF.

Problem #8 (Flip-Flop, 25 points).

The following schematic shows a D flip-flop. CK is the clock input, Q is the output, and D is the data input signal. Answer the following questions.



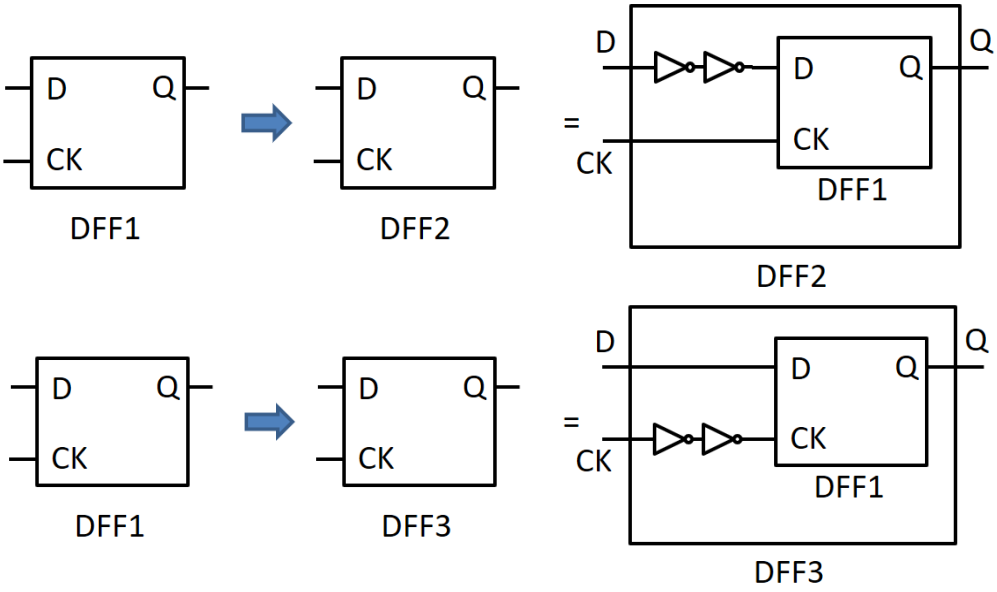
(1) Is it positive-edge-triggered or negative-edge-triggered?

(2) Explain how you can estimate the setup time of the FF.

(3) Explain how you can estimate the hold time of the FF.

Problem #9 (Flip-Flop, 20 points).

Suppose a D-FF design is given (DFF1) as shown below. Now, we design a new D-FF (DFF2) using a DFF1 as follows. DFF2 has two inverters between the input pin D of DFF2 and the input pin D of DFF1. Similarly, we design a new D-FF (DFF3) using a DFF1 as shown below. Notice that users of DFF2 and DFF3 cannot see the internal designs of DFF2 and DFF3.



- Hold time and setup time of DFF1: h_1 and s_1, respectively
- Hold time and setup time of DFF2: h_2 and s_2, respectively
- Hold time and setup time of DFF3: h_3 and s_3, respectively
- The delay of an inverter: d
- Clock period: T (duty cycle: 50%)

(1) Express h_2 as a function of h_1, s_1, d, T.

(2) Express s_2 as a function of h_1, s_1, d, T.

(3) Express h_3 as a function of h_1, s_1, d, T.

(4) Express s_3 as a function of h_1, s_1, d, T.