EE466

VLSI System Design

Midterm Exam

Oct. 15, 2020. (4:20pm – 5:35pm)

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Name:

WSU ID:

Problem	Points	
1	10	
2	10	
3	10	
4	10	
5	10	
6	10	
Total	60	

* Allowed: Textbooks, cheat sheets, class notes, notebooks, calculators, watches

* Not allowed: Electronic devices (smart phones, tablet PCs, laptops, etc.) except calculators and watches

Problem #1 (Kogge-Stone Adder, 10 points).

For the 1024-bit Kogge-Stone adder, show one of the critical paths to calculate S_{789}.

Problem #2 (Carry-Lookahead Adder, 10 points).

For the 1024-bit Carry-lookahead adder, show one of the critical paths to calculate S_{789}.

Problem #3 (Conditional Sum Adder, 10 points)

How many 1-bit multiplexers do we need to implement a 64-bit conditional sum adder? (do not assume that C_0 is 0. C_0 could be 0 or 1.)

Problem #4 (Carry Skip Adder, 10 points)

For the 64-bit Carry-skip adder, show how S_{33} is generated from the primary input signals. Assume that the 4-bit blocks in the carry-skip adder are 4-bit ripple-carry adders with a separate logic generating $g_{i+3:i}$ and $p_{i+3:i}$ (i.e., the sum bits are generated purely by ripple-carry adders when C_{4k} is available). For the output Y of a two-input MUX (S: selection, J: input selected for $S = 0$, K: input selected for $S = 1$), you can use the following Boolean equation: $Y = \bar{S} \cdot J + S \cdot K$.

Problem #5 (Carry Select Adder, 10 points)

We want to design an n-bit adder. The top-level architecture of the n-bit adder is the carry select adder architecture and is divided into $\frac{n}{m}$ groups and we use m-bit adders in each group. Now, we design the m-bit adders using the carry select adder architecture again. Each m-bit adder is divided into $\frac{m}{k}$ groups and we use k-bit adders in each group. (Thus, it is a recursively-designed carry select adder). The k-bit adders are ripple-carry adders. For the carry-out logic, we use a two-input MUX.

Express the worst-case delay as a function of n, m, k, d, e where d is the delay of a full adder and e is the delay of a two-input MUX. (See page 8 and 9 in the lecture note.)

Problem #6 (Modified Booth Encoding, 10 points)

Use the modified Booth encoding technique to calculate the following multiplication (see page 9 in the multiplier lecture notes). Assume that all the numbers are unsigned.

$$
\begin{array}{ll}
A & 1\,0\,1\,0\,1\,1\,1\,0 \\
*\,X & 1\,0\,1\,0\,1\,1\,0\,1 \\
\hline
\end{array}
$$