EE466

VLSI System Design

Midterm Exam 2

Nov. 17, 2020. (4:20pm – 5:35pm)

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Name:

WSU ID:

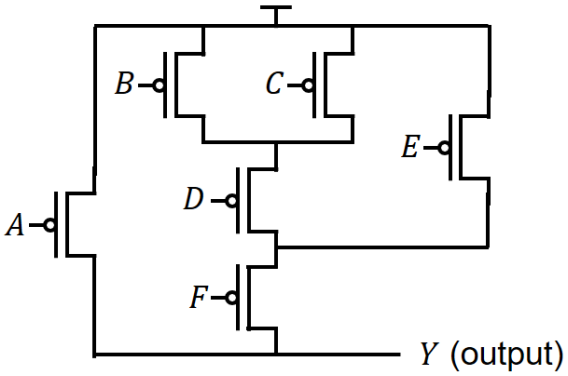
Problem	Points	
1	10	
2	10	
3	10	
4	10	
5	10	
Total	50	

* Allowed: Textbooks, cheat sheets, class notes, notebooks, calculators, watches

* Not allowed: Electronic devices (smart phones, tablet PCs, laptops, etc.) except calculators and watches

Problem #1 (Static CMOS Logic, 10 points).

The following shows the PFET network of a logic gate designed by the static CMOS design methodology. Design the NFET network of the gate (i.e., draw a transistor-level schematic of the NFET network).



Problem #2 (Static CMOS Logic, 10 points).

Design the following logic gate using the static CMOS logic design methodology.

$$Y = (\overline{A \cdot B + C}) \cdot (D + E)$$

Available inputs: A, B, C, D, E. Try to minimize # TRs.

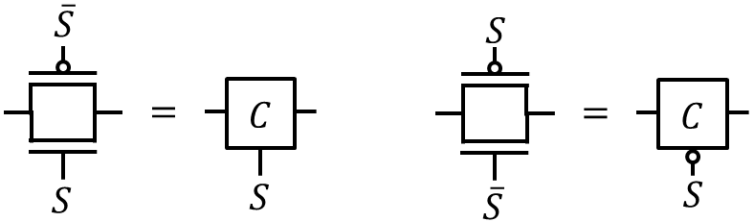
Problem #3 (Transmission Gates, 10 points).

Design the following logic gate using transmission gates (TGs).

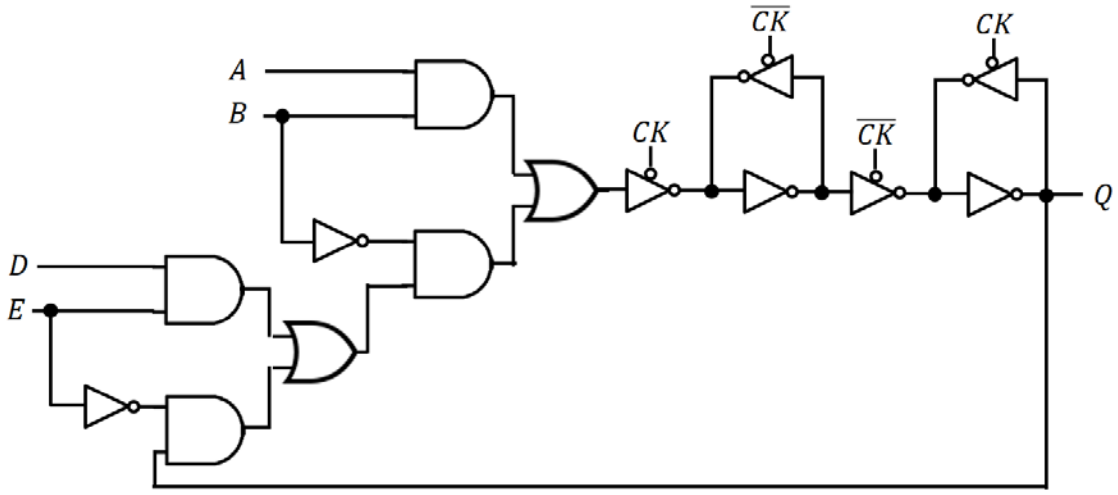
$$Y = (\overline{A \cdot B + C}) \cdot (D + E)$$

Available inputs: A, B, C, D, E (and VDD and GND). Use the following symbols for the TGs.

≤12 TGs: 10 points. ≤14 TGs: 7 points. ≤16 TGs: 5 points. Otherwise: 3 points.



Problem #4 (Logic Analysis, 10 points).



This logic gate is a flip-flop (D is a data input, CK is a clock input, and A, B, E are some additional inputs.) Describe the functionality of the flip-flop in as much detail as possible (e.g., whether it is positive-edge-triggered, negative-edge-triggered, or dual-edge, and what A does, etc.).

Problem #5 (Static CMOS Logic, 10 points).

This logic gate is a sequential logic (D is a data input, CK is a clock input, and A, B are some additional inputs.) Describe the functionality of the gate in as much detail as possible.