EE434

ASIC and Digital Systems

Midterm Exam 1

Feb. 26, 2021. (2:10pm – 3pm)

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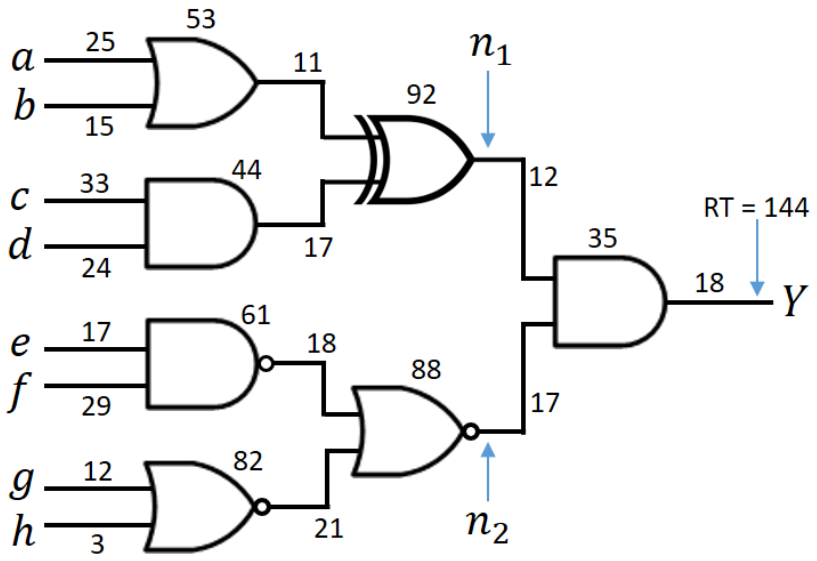
Name:

WSU ID:

Problem	Points	
1	10	
2	40	
3	40	
4	40	
Total	130	

Problem #1 (STA, 10 points)

The following figure shows the delays (in ps) of the gates and nets of a logic design. The required time (RT) at the output node Y is 144 ps. All the inputs have zero arrival time.



1) Calculate the slack at node n_1.

AT: MAX(MAX(25, 15) + 53 + 11, MAX(33, 24) + 44 + 17) + 92 = MAX(89, 94) + 92 = 186ps

RT: 144 – 18 – 35 – 12 = 79ps

Slack: 79 – 186 = -107ps

2) Calculate the slack at node n_2.

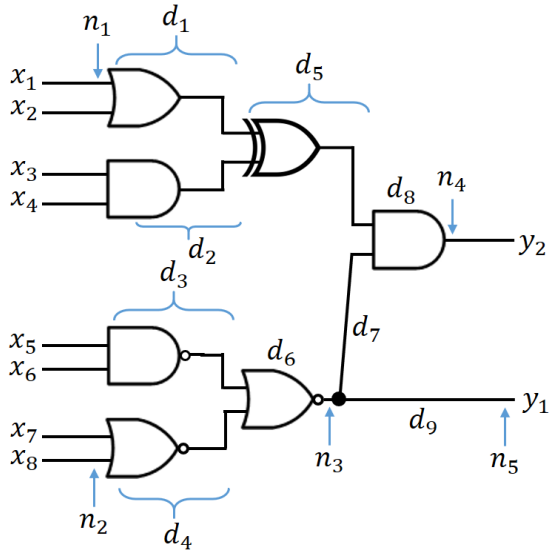
AT: MAX(MAX(17, 29) + 61 + 18, MAX(12, 3) + 82 + 21) + 88 = MAX(108, 115) + 88 = 203ps

RT: 144 – 18 – 35 – 17 = 74ps

Slack: 74 – 203 = -129ps

Problem #2 (STA, 40 points)

The following figure shows a logic design. x_k's are input signals and y_k's are output signals. The slack at node n_k is denoted by s_k. Notice that the gates and nets have some delays. The inputs have the same arrival time a and the outputs have the same required time r.



1) Prove or disprove that $s_1 \geq s_4$ is always true.

Denote the AT and RT at node n_k by a_k and r_k, respectively.

$S = s_4 - s_1 = (r_4 - a_4) - (r_1 - a_1) = (r_4 - r_1) - (a_4 - a_1)$.

$r_1 = r_4 - d_8 - d_5 - d_1$, so $r_4 - r_1 = d_1 + d_5 + d_8$.

$a_4 = MAX(a_{top}, a_{bot}) + d_8$ where a_{top} and a_{bot} are the ATs of the top and bottom nodes of the AND gate before n_4. Then, $a_4 \geq a_{top} + d_8$ is true. Notice that $a_{top} \geq a_1 + d_1 + d_5$. Thus, $a_4 \geq a_1 + d_1 + d_5 + d_8$, or I can rewrite it as $a_4 = a_1 + d_1 + d_5 + d_8 + e$ where $e \geq 0$. Then, $a_4 - a_1 = d_1 + d_5 + d_8 + e$.

Now, $S = (d_1 + d_5 + d_8) - (d_1 + d_5 + d_8 + e) = -e$, so $S = -e \leq 0$, so $s_4 \leq s_1$.

Intuitively speaking, if n_1 has the worst slack than all the other nodes, the slack is propagated to the outputs.

2) Prove or disprove that $s_2 \geq s_4$ is always true.

If n2-n3-n5 is the critical path, $s_2 < s_4$, so it is not true.

3) Prove or disprove that $s_3 \geq s_4$ is always true.

For the same reason, $s_3 < s_4$ can happen.

4) Prove or disprove that $s_4 \geq s_5$ is always true.

$$S = s_5 - s_4 = (r_5 - r_4) - (a_5 - a_4).$$

$r_4 = r_5 - y$ (y is the delay of the net between n_4 and y_2, $y \geq 0$).

$r_5 - r_4 = y$.

$a_5 = a_3 + d_9$.

$a_4 = MAX(a_3 + d_7, a_8) + d_8$ where a_8 is the arrival time at the top input of the AND gate whose delay is d_8.

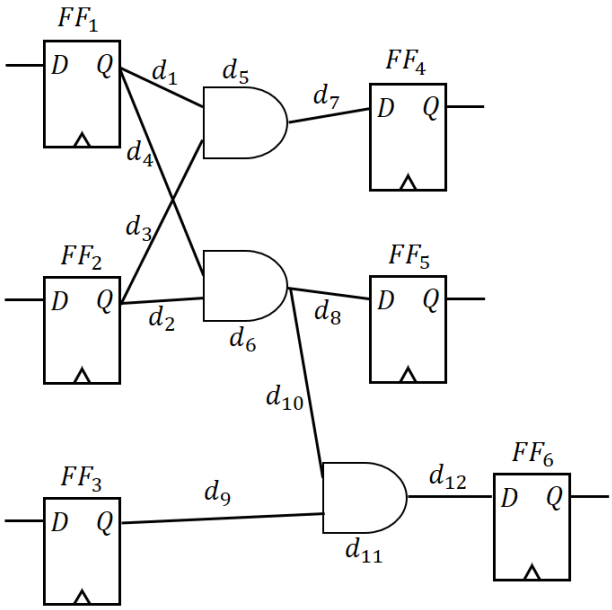
$a_5 - a_4 = a_3 + d_9 - MAX(a_3 + d_7, a_8) - d_8$.

Thus, $S = y + d_8 - d_9 + MAX(a_3 + d_7, a_8) - a_3$.

Depending on the delay values, S could be negative, zero, or positive. Thus, it is not true.

Problem #3 (Setup and Hold Time, 40 points)

The following figure shows a part of a design.



- d_k: delay ($k = 1\sim12$)
- s_k: setup time of FF_k ($k = 1\sim6$)
- h_k: hold time of FF_k ($k = 1\sim6$)
- x_k: delay from the clock source to the clock pin of FF_k ($k = 1\sim6$)
- c_k: clk-to-Q delay of FF_k ($k = 1\sim6$)
- T_{CLK}: clock period
- MIN, MAX: MIN, MAX operators

1) Derive a setup time constraint (inequality) for the signals coming to the input of FF_4.

$$MAX(x_1 + c_1 + d_1, x_2 + c_2 + d_3) + d_5 + d_7 \leq x_4 + T_{CLK} - s_4$$

2) Derive a hold time constraint (inequality) for the signals coming to the input of FF_4.

$$MIN(x_1 + c_1 + d_1, x_2 + c_2 + d_3) + d_5 + d_7 \geq x_4 + h_4$$

3) Express the slack at the input pin D of FF_5 as a function of the constants above.

$$RT = x_5 + T_{CLK} - s_5$$

$$AT = MAX(x_1 + c_1 + d_4, x_2 + c_2 + d_2) + d_6 + d_8$$

$$Slack = RT - AT = x_5 + T_{CLK} - s_5 - MAX(x_1 + c_1 + d_4, x_2 + c_2 + d_2) - d_6 - d_8$$

4) Express the slack at the output pin Q of FF_3 as a function of the constants above.

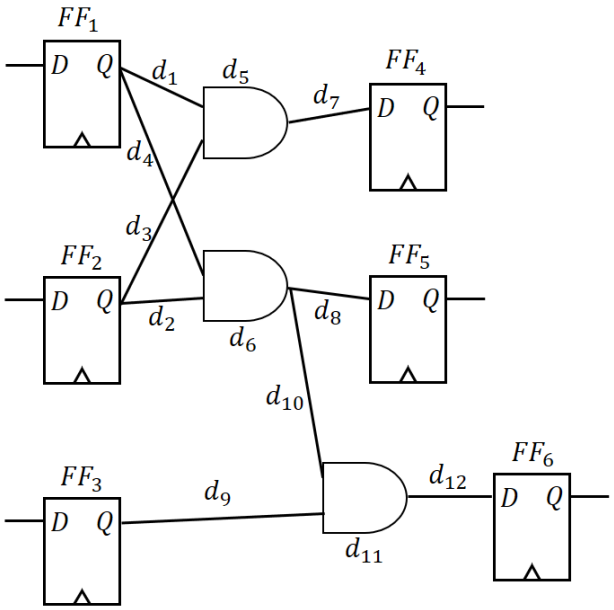
$$RT = x_6 + T_{CLK} - s_6 - d_{12} - d_{11} - d_9$$

$$AT = x_3 + c_3$$

$$Slack = x_6 + T_{CLK} - s_6 - d_{12} - d_{11} - d_9 - x_3 - c_3$$

Problem #4 (Setup and Hold Time, 40 points)

The following figure shows a part of a design.



- d_k: delay ($k = 1\sim12$)
- $S(FF_k, D)$: Slack at the input pin D of FF_k

Assume that all the flip-flops have the same setup time s, the same hold time h, the same clock-to-Q delay c, and the same delay x from the clock source to the clock pins.

Answer the following questions.

(Correct: +4 points, No answer: 0 point, Wrong: -2 points)

1) It is possible that FF_5 satisfies its setup time constraint while FF_6 violates its setup time constraint. (**True** / False)

The path from FF_3 to FF_6 could violate the setup time constraint.

2) It is possible that FF_5 satisfies its setup time constraint while FF_6 violates its hold time constraint. (**True** / False)

The path from FF_3 to FF_6 could violate the hold time constraint.

3) It is possible that FF_5 satisfies its hold time constraint while FF_6 violates its setup time constraint. (**True** / False)

The path from FF_3 to FF_6 could violate the setup time constraint.

4) It is possible that FF_5 satisfies its hold time constraint while FF_6 violates its hold time constraint. (**True** / False)

The path from FF_3 to FF_6 could violate the hold time constraint.

5) It is possible that FF_5 violates its setup time constraint while FF_6 satisfies its setup time constraint. (**True** / False)

If d_8 is large, FF_5 violates its setup time constraint, but the path to FF_6 can still satisfy the setup time constraint.

6) It is possible that FF_5 violates its setup time constraint while FF_6 satisfies its hold time constraint. (**True** / False)

If d_8 is large, FF_5 violates its setup time constraint, but the path to FF_6 can still satisfy the hold time constraint.

7) It is possible that FF_5 violates its hold time constraint while FF_6 satisfies its setup time constraint. (**True** / False)

8) It is possible that FF_5 violates its hold time constraint while FF_6 satisfies its hold time constraint. (**True** / False)

9) If d_4 goes down, $S(FF_6, D)$ goes up. (True / **False**)

If FF_3 to FF_6 is the critical path, $S(FF_6, D)$ doesn't go up even if d_4 goes down.

10) If d_9 goes down, $S(FF_6, D)$ goes up. (True / **False**)