EE434

ASIC and Digital Systems

Midterm Exam 1

Feb. 26, 2021. (2:10pm – 3pm)

Instructor: Dae Hyun Kim (daehyun@eecs.wsu.edu)

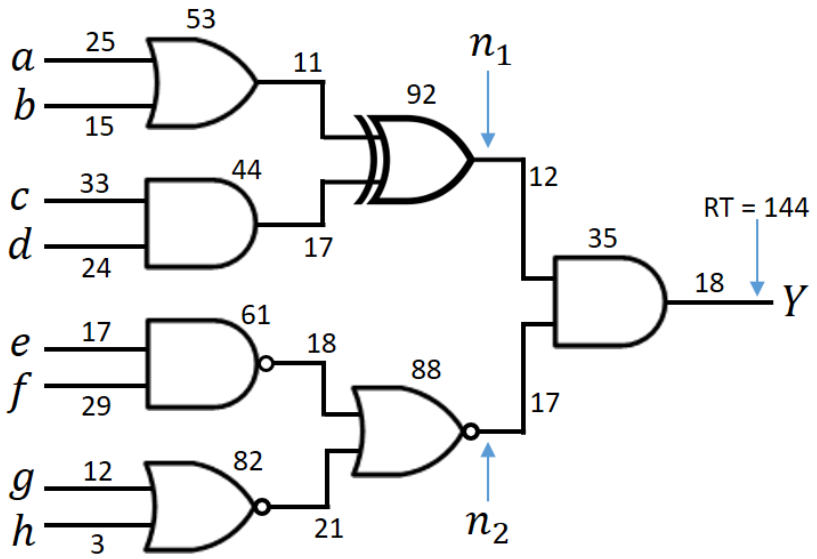
Name:

WSU ID:

Problem	Points	
1	10	
2	40	
3	40	
4	40	
Total	130	

Problem #1 (STA, 10 points)

The following figure shows the delays (in ps) of the gates and nets of a logic design. The required time (RT) at the output node Y is 144 ps. All the inputs have zero arrival time.

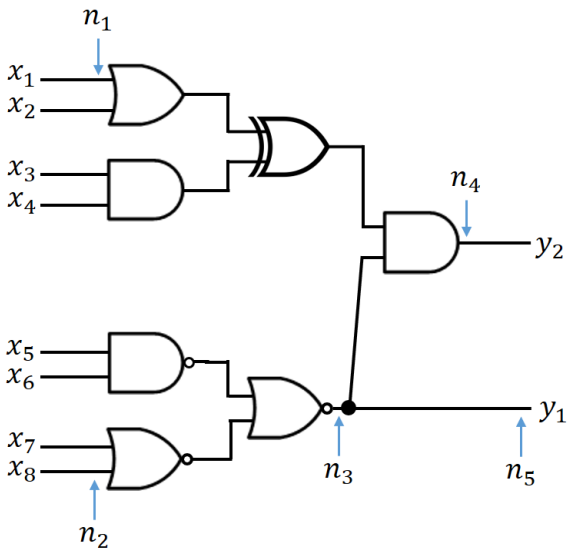


1) Calculate the slack at node n_1.

2) Calculate the slack at node n_2.

Problem #2 (STA, 40 points)

The following figure shows a logic design. x_k's are input signals and y_k's are output signals. The slack at node n_k is denoted by s_k. Notice that the gates and nets have some delays. The inputs have the same arrival time a and the outputs have the same required time r.



1) Prove or disprove that $s_1 \geq s_4$ is always true.

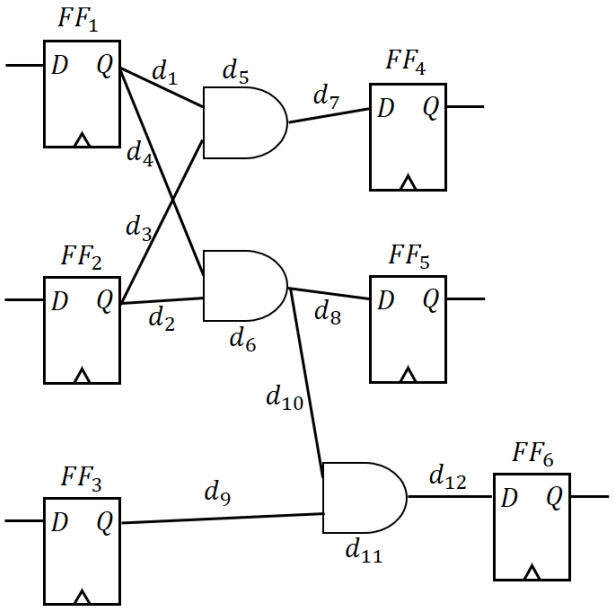
2) Prove or disprove that $s_2 \geq s_4$ is always true.

3) Prove or disprove that $s_3 \geq s_4$ is always true.

4) Prove or disprove that $s_4 \geq s_5$ is always true.

Problem #3 (Setup and Hold Time, 40 points)

The following figure shows a part of a design.



- d_k: delay ($k = 1\sim12$)
- s_k: setup time of FF_k ($k = 1\sim6$)
- h_k: hold time of FF_k ($k = 1\sim6$)
- x_k: delay from the clock source to the clock pin of FF_k ($k = 1\sim6$)
- c_k: clk-to-Q delay of FF_k ($k = 1\sim6$)
- T_{CLK}: clock period
- MIN, MAX: MIN, MAX operators

1) Derive a setup time constraint (inequality) for the signals coming to the input of FF_4.

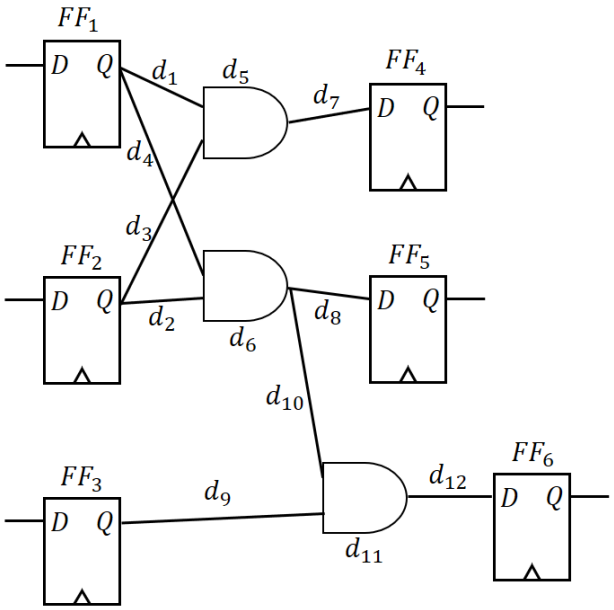
2) Derive a hold time constraint (inequality) for the signals coming to the input of FF_4.

3) Express the slack at the input pin D of FF_5 as a function of the constants above.

4) Express the slack at the output pin Q of FF_3 as a function of the constants above.

Problem #4 (Setup and Hold Time, 40 points)

The following figure shows a part of a design.



- d_k: delay ($k = 1\sim12$)
- $S(FF_k, D)$: Slack at the input pin D of FF_k

Assume that all the flip-flops have the same setup time s, the same hold time h, the same clock-to-Q delay c, and the same delay x from the clock source to the clock pins.

Answer the following questions.

(Correct: +4 points, No answer: 0 point, Wrong: -2 points)

1) It is possible that FF_5 satisfies its setup time constraint while FF_6 violates its setup time constraint. (True / False)

2) It is possible that FF_5 satisfies its setup time constraint while FF_6 violates its hold time constraint. (True / False)

3) It is possible that FF_5 satisfies its hold time constraint while FF_6 violates its setup time constraint. (True / False)

4) It is possible that FF_5 satisfies its hold time constraint while FF_6 violates its hold time constraint. (True / False)

5) It is possible that FF_5 violates its setup time constraint while FF_6 satisfies its setup time constraint. (True / False)

6) It is possible that FF_5 violates its setup time constraint while FF_6 satisfies its hold time constraint. (True / False)

7) It is possible that FF_5 violates its hold time constraint while FF_6 satisfies its setup time constraint. (True / False)

8) It is possible that FF_5 violates its hold time constraint while FF_6 satisfies its hold time constraint. (True / False)

9) If d_4 goes down, $S(FF_6, D)$ goes up. (True / False)

10) If d_9 goes down, $S(FF_6, D)$ goes up. (True / False)