EE434

ASIC and Digital Systems

Midterm Exam 2

Apr. 7, 2021. (2:10pm – 3pm)

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Name:

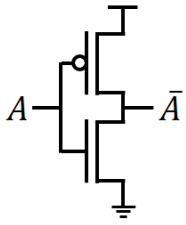
WSU ID:

Problem	Points	
1	10	
2	10	
3	15	
4	10	
5	10	
6	15	
Total	70	

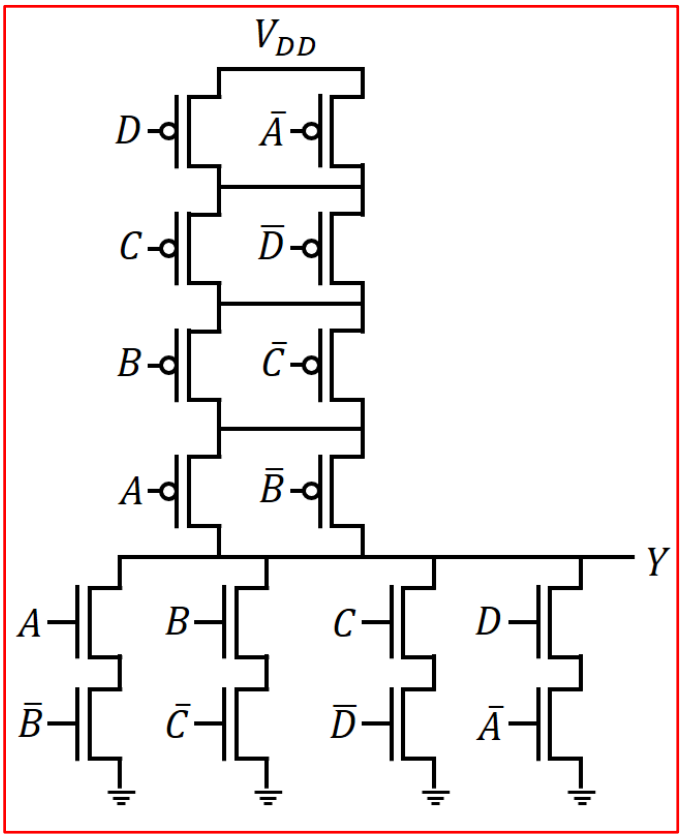
Problem #1 (Static CMOS, 10 points)

Design the following function (draw a transistor-level schematic) using the static CMOS logic design methodology. Available input: A, B, C, D. # TRs should be less than or equal to 24.

$$Y = \overline{A \cdot \bar{B} + B \cdot \bar{C} + C \cdot \bar{D} + D \cdot \bar{A}}$$



(same for B, C, D)

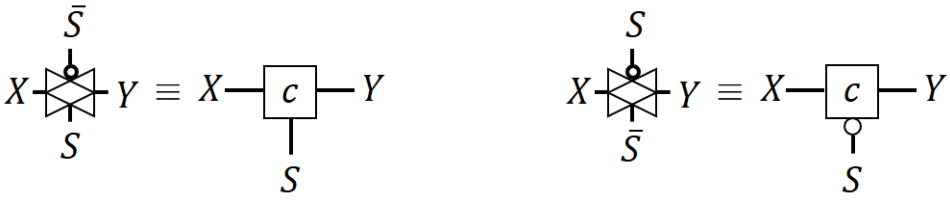


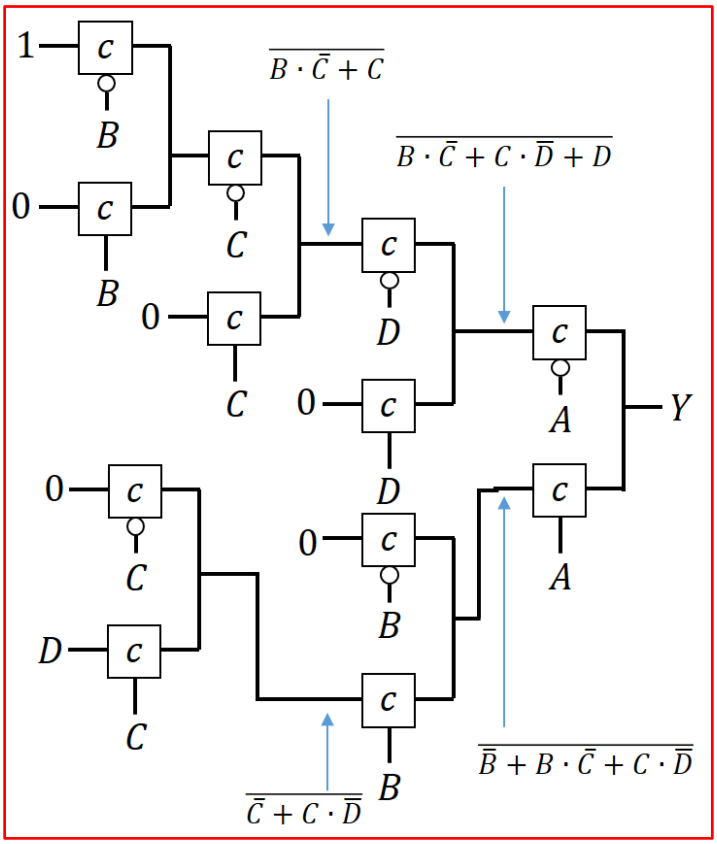
Problem #2 (Transmission Gates, 10 points)

Design the following function (draw a transmission-gate-level schematic) using transmission gates only. Available input: $A, B, C, D, 0\ (GND), 1\ (VDD)$.

$$Y = \overline{A \cdot \bar{B} + B \cdot \bar{C} + C \cdot \bar{D} + D \cdot \bar{A}}$$

You can use the following symbols for transmission gates.

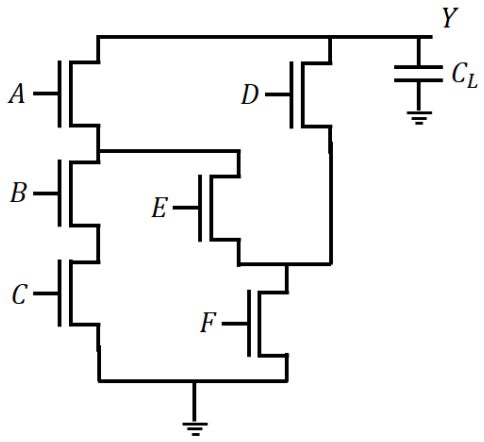




Problem #3 (TR Sizing, 15 points)

Size the transistors in the following schematic to satisfy the given timing constraint.

- R_n: The resistance of a 1X NFET.
- The delay should be $\leq R_n C_L$.
- Try to minimize the total transistor width.



1) (10 points) Size the transistors. You will get 10 points if the total TR width is $\leq$ 22X.

A: 2 X

B: 4 X

C: 4 X

D: 4 X

E: 4 X

F: 4 X

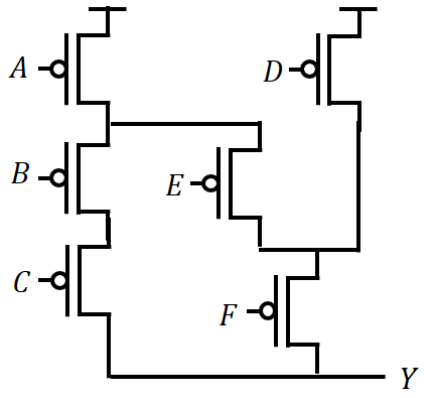
If the total TR width you obtained above is less than 22X, you don't need to solve the second problem. You will get 15 points. If the width is greater than 22X, you don't need to solve the second problem. You won't get the extra points. If the width is 22X, solve the second problem.

2) (5 points) In your solution, you can upsize only one TR (and of course downsize all the other TRs as a result) to reduce the total TR width further. Which TR do you want to upsize?

Transistor E.

Problem #4 (Logic Analysis, 10 points)

The following shows the PFET network of a static CMOS logic gate. Express the output Y as a Boolean function of the input variables A, B, C, D, E, F.



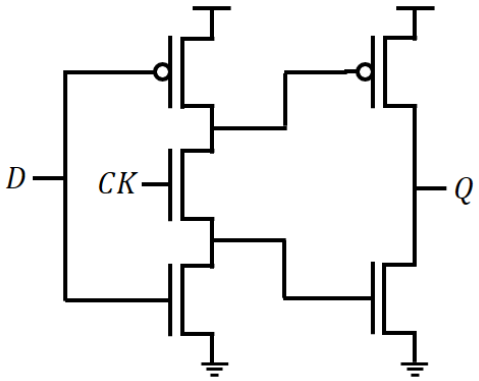
(You don't need to simplify the expression.)

Y becomes 1 when A=B=C=0 or A=E=F=0 or B=C=D=E=0 or D=F=0.

$$Y = \bar{A} \cdot (\bar{B} \cdot \bar{C} + \bar{E} \cdot \bar{F}) + \bar{D} \cdot (\bar{B} \cdot \bar{C} \cdot \bar{E} + \bar{F})$$

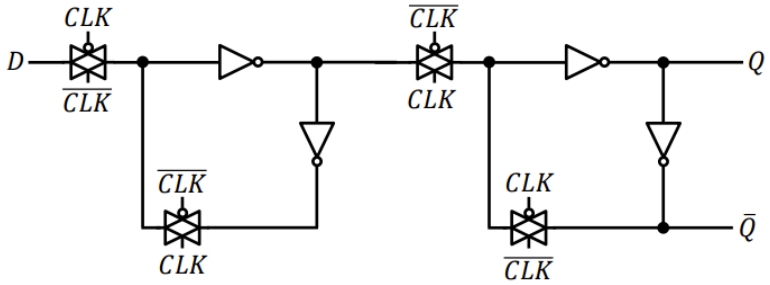
Problem #5 (Logic Analysis, 10 points)

What does the following circuit do? Describe its functionality in as much detail as possible. (D: data input. CK: clock. Q: data output)



This is a positive-edge-triggered D flip-flop.

Problem #6 (Logic Design, 15 points)



This is a positive-edge-triggered D flip-flop (FF). Can you modify the design (add some logic gates such as AND and OR to the design and/or remove some gates from the design, etc.) and add a control signal R to the design so that you can reset the D FF? Here is a more detailed description of the behavior of the logic.

- If $R = 1$, Q becomes 0 immediately regardless of D and CLK.
- If R switches from 1 to 0, Q should still be 0 until the next clock rising edge.