EE434

ASIC and Digital Systems

Final Exam

May 5, 2022. (1:30pm – 3:30pm)

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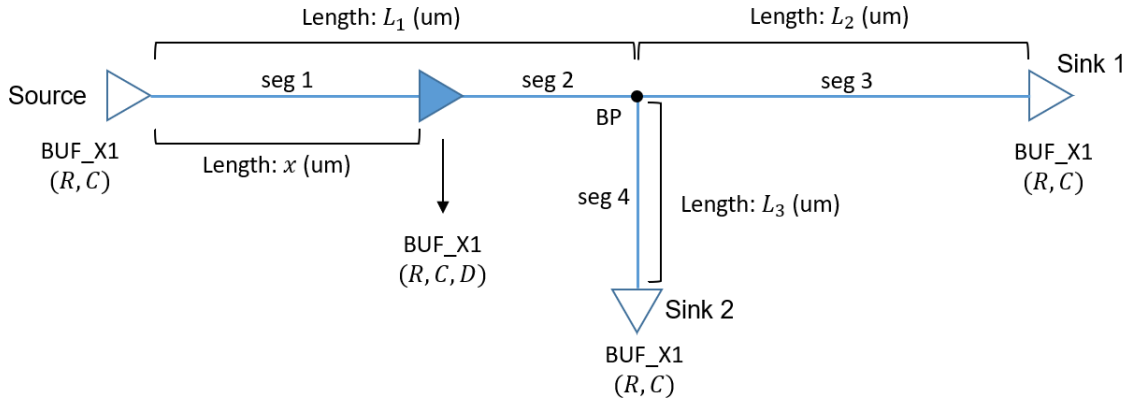
Name:

WSU ID:

Problem	Points	
1	80	
2	80	
3	50	
4	50	
Total	260	

Problem #1 (Interconnect Optimization, 80 points)

The following figure shows a net optimized by a buffer.



Constants

- Output resistance of a cell: R
- Input capacitance of a cell: C
- Internal delay of a buffer: D
- Unit wire resistance and capacitance: r (Ω/um), c (fF/um)
- Length of each subnet: L_1, L_2, L_3 (um)

Independent variable

- Location of the buffer: x $(0 < x < L_1)$

We want to optimize the delay from the driver to Sink 1 or Sink 2. "BP" is a branch point. Answer the following questions.

(1) Replace each segment (seg 1, 2, 3, 4) by a PI model. Then, express the delay from the source to Sink 1 using the Elmore delay model. (10 points)

$$\tau = rL_2\left(\frac{cL_2}{2} + C\right) + r(L_1 - x)\left(\frac{c(L_1 - x)}{2} + cL_2 + cL_3 + 2C\right)$$
$$+ R(c(L_1 - x) + cL_2 + cL_3 + 2C) + D + rx\left(\frac{cx}{2} + C\right) + R(cx + C)$$

(2) Find the optimal location (x) of the buffer minimizing the delay from the source to Sink 1. (10 points)

$$\frac{d\tau}{dx} = Rc + rcx + rC - Rc + rc(x - L_1) - r(cL_2 + cL_3 + 2C) = 0$$

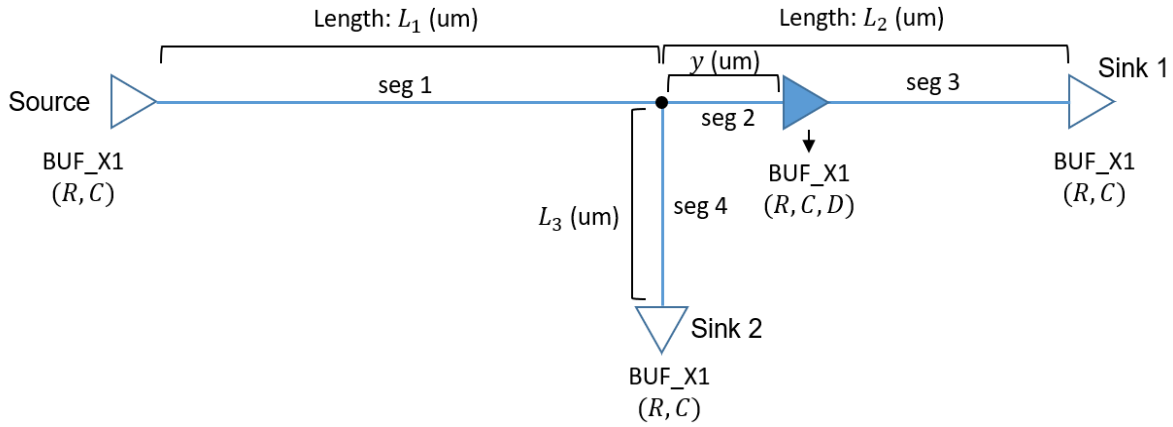
$$2cx = c(L_1 + L_2 + L_3) + C$$

$$\therefore x = \frac{1}{2}(L_1 + L_2 + L_3) + \frac{C}{2c}$$

(3) Answer the following questions for the problems (1)-(2) (Correct: +4 points, Wrong: -4 points, No answer: 0) for the minimization of the delay from the source to Sink 1.

- If L_1 increases, x increases. (**True** / False)
- If L_2 increases, x increases. (**True** / False)
- If L_3 increases, x increases. (**True** / False)
- If C (the input capacitance of a cell) increases, x increases. (**True** / False)
- If c (the unit wire capacitance) increases, x increases. (True / **False**)

Now, we are moving the buffer to the branch connected to Sink 1 as follows:



(4) Replace each segment (seg 1, 2, 3, 4) by a PI model. Then, express the delay from the source to Sink 1 using the Elmore delay model. (10 points)

$$\tau = r(L_2 - y)\left(\frac{c(L_2 - y)}{2} + C\right) + R(c(L_2 - y) + C) + D + ry\left(\frac{cy}{2} + C\right)$$
$$+ rL_1\left(\frac{cL_1}{2} + cy + cL_3 + 2C\right) + R(cL_1 + cy + cL_3 + 2C)$$

(5) Find the optimal location (y) of the buffer minimizing the delay from the source to Sink 1. (10 points)

$$\frac{d\tau}{dy} = Rc + rcL_1 + rcy + rC - Rc + rc(y - L_2) - rC = 0$$

$$2cy = c(L_2 - L_1)$$

$$\therefore y = \frac{1}{2}(L_2 - L_1)$$

(6) Answer the following questions for the problems (4)-(5) (Correct: +5 points, Wrong: -5 points, No answer: 0) for the minimization of the delay from the source to Sink 1.

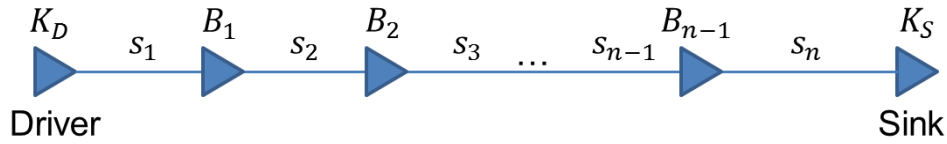
- If L_1 increases, y increases. (True / **False**)
- If L_2 increases, y increases. (**True** / False)

(7) Replace each segment (seg 1, 2, 3, 4) by a PI model. Then, express the delay from the source to Sink 2 using the Elmore delay model. (10 points)

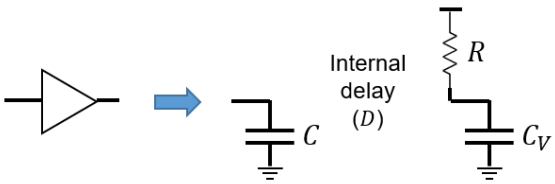
$$\tau = rL_3\left(\frac{cL_3}{2} + C\right) + rL_1\left(\frac{cL_1}{2} + cL_3 + cy + 2C\right) + R(cL_1 + cL_3 + y + 2C)$$

Problem #2 (Interconnect Optimization, 80 points)

The following figure shows a net optimized by buffer insertion. The driver and the sink are denoted by K_D and K_S, respectively, and the inserted buffers are denoted by B_i ($1 \leq i \leq n-1$). $n \geq 2$, i.e., there is at least one buffer between the driver and the sink.



- Output resistance of a cell (K_D and B_i): R
- Input capacitance of a cell (K_S and B_i): C
- Delay of a buffer: D
- Length of the i-th net ($1 \leq i \leq n$): s_i (um)
- $\sum_{i=1}^{n} s_i = L$ (um)
- Unit wire resistance and capacitance: r (Ω/um), c (fF/um)
- Use the PI model to model each segment.
- Use the following model to model a cell (the driver, the sink, and the buffers). (Notice that there is an output capacitor with capacitance C_V.)



(1) Find the optimal locations of the buffers (i.e., express s_i as a function for the given parameters for each $i = 1,2,\dots,n$) minimizing the delay from the driver to the sink. (20 points)

$$\tau_i = R(C_V + cs_i + C) + rs_iC + \frac{1}{2}rcs_i^2$$

$$\tau = \sum \tau_i = nR(C_V + C) + RcL + rCL + \frac{1}{2}rc\left(\sum s_i^2\right) + (n-1)D$$

$$\frac{\partial \tau}{\partial s_i} = rcs_i + rc\big(L - (s_1 + \cdots + s_{n-1})\big)(-1) = 0, \therefore s_i = L - (s_1 + \cdots + s_{n-1})$$

$$\therefore s_1 = \cdots = s_{n-1}, \boldsymbol{s_i = \frac{L}{n}}$$

(2) Then, find the optimal # buffers (n) minimizing the delay (express n as a function of the given parameters). (20 points)

$$\tau = \sum \tau_i = nR(C_V + C) + RcL + rCL + \frac{1}{2}rc\frac{L^2}{n} + (n-1)D$$

$$\frac{\partial \tau}{\partial n} = R(C_V + C) - \frac{1}{2}rc\frac{L^2}{n^2} + D = 0$$

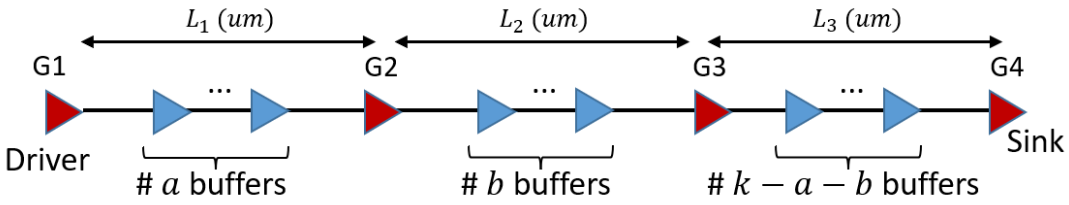
$$n = \sqrt{\frac{rcL^2}{2\{R(C_V + C) + D\}}}$$

(3) Answer the following questions for the problem (1) (Correct: +4 points, Wrong: -4 points, No answer: 0) for the minimization of the delay from the driver to the sink.

- If L increases, n increases. (True / False)
- If r increases, n increases. (True / False)
- If c increases, n increases. (True / False)
- If R increases, n increases. (True / False)
- If C increases, n increases. (True / False)
- If C_V increases, n increases. (True / False)
- If D increases, n increases. (True / False)
- If the output capacitance (C_V) of B_{n-1} increases, s_n increases. (True / False)
- If the output capacitance (C_V) of B_{n-1} increases, s_{n-1} increases. (True / False)
- If the output capacitance (C_V) of B_{n-1} increases, s_1 increases. (True / False)

Problem #3 (Interconnect Optimization, 50 points)

The following shows three nets connecting four gates (G_1, G_2, G_3, G_4). To reduce the delay, you insert buffers between G_1 and G_2, between G_2 and G_3, and between G_3 and G_4. The total number of buffers you insert is k (constant). Thus, the total # of buffers you insert between G_1 and G_2 is a, the total # buffers you insert between G_2 and G_3 is b, and total # buffers you insert between G_3 and G_4 is $k - a - b$.



- All the gates and buffers are of the same type (they have the same output resistance, input capacitance, and internal delay). You can ignore the output capacitance of each gate.

(1) Find a and b minimizing the delay from the driver to the sink. (30 points)

First of all, if we insert t number of buffers into a net, we should evenly distribute them to minimize the delay (notice that all the gates are of the same type). Thus, if we insert a buffers into the first net, its delay is

$$\tau_1 = (a+1)\left\{R\left(c\frac{L_1}{a+1} + C\right) + r\frac{L_1}{a+1}C + \frac{1}{2}rc\left(\frac{L_1}{a+1}\right)^2\right\} + aD$$

Similarly, if we insert b buffers into the second net, its delay is

$$\tau_2 = (b+1)\left\{R\left(c\frac{L_2}{b+1} + C\right) + r\frac{L_2}{b+1}C + \frac{1}{2}rc\left(\frac{L_2}{b+1}\right)^2\right\} + bD$$

The delay of the third net is

$$\tau_3 = (k-a-b+1)\left\{R\left(c\frac{L_3}{k-a-b+1} + C\right) + r\frac{L_3}{k-a-b+1}C + \frac{1}{2}rc\left(\frac{L_3}{k-a-b+1}\right)^2\right\} + (k-a-b)D$$

Thus, the total delay is

$$\tau = \tau_1 + \tau_2 + \tau_3$$

$$= RcL_1 + RC(a+1) + rL_1C + \frac{1}{2}rc\frac{{L_1}^2}{a+1} + RcL_2 + RC(b+1) + rL_2C$$

$$+ \frac{1}{2}rc\frac{{L_2}^2}{b+1} + RcL_3 + RC(k-a-b+1) + rL_3C + \frac{1}{2}rc\frac{{L_3}^2}{k-a-b+1} + kD$$

$$= RcL + RC(k+3) + rcL + kD + \frac{1}{2}rc\left\{\frac{{L_1}^2}{a+1} + \frac{{L_2}^2}{b+1} + \frac{{L_3}^2}{k-a-b+1}\right\}$$

where $(L = L_1 + L_2 + L_3)$

$\frac{\partial\tau}{\partial a} = 0$ => $-\frac{{L_1}^2}{(a+1)^2} + \frac{{L_3}^2}{(k-a-b+1)^2} = 0$

$\frac{\partial\tau}{\partial b} = 0$ => $-\frac{{L_2}^2}{(b+1)^2} + \frac{{L_3}^2}{(k-a-b+1)^2} = 0$

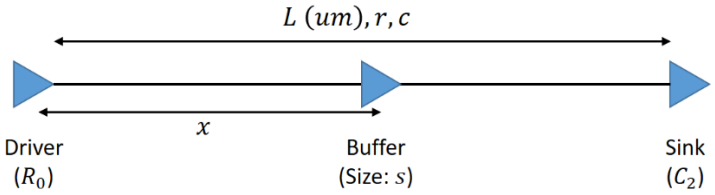
$$a = \frac{(k+2)L_1 - L_2 - L_3}{L_1 + L_2 + L_3}$$

$$b = \frac{(k+2)L_2 - L_1 - L_3}{L_1 + L_2 + L_3}$$

(2) Answer the following questions for the problem (1) (Correct: +5 points, Wrong: -5 points, No answer: 0) for the minimization of the delay from the driver to the sink.

- If k increases, a increases. (True / False)
- If k increases, b increases. (True / False)
- If the input capacitance of the sink increases, a increases. (True / False)
- If the input capacitance of the sink increases, b increases. (True / False)

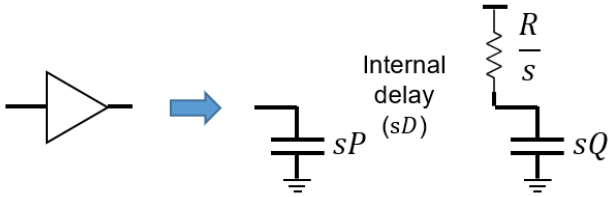
Problem #4 (Interconnects, 40 points)



The figure shows a long wire whose length, unit resistance and capacitance are L, r, and c, respectively. We want to insert a buffer ($0 < x < L$). The size of the buffer is s and its output resistance, input capacitance, output capacitance, and internal delay are as follows:

- Output resistance: $\frac{R}{s}$ (where R is a constant)
- Input capacitance: sP (where P is a constant)
- Output capacitance: sQ (where Q is a constant)
- Internal delay: sD (where D is a constant)

R_0 is the output resistance of the driver and C_2 is the input capacitance of the sink. Notice that there are two variables, x and s. You can model the buffer using the following model.



(1) Express the total delay as a function of the variables and the constants. (10 points)

$$\tau = R_0(cx + sP) + rxsP + \frac{1}{2}rcx^2 + sD + \frac{R}{s}(sQ + c(L - x) + C_2) + r(L - x)C_2 + \frac{1}{2}rc(L - x)^2$$

(2) Find the optimal location of the buffer (you can treat s as a constant.) (10 points)

$$\frac{\partial \tau}{\partial x} = R_0 c + rsP + rcx - \frac{RC}{s} - rC_2 + rc(x - L) = 0$$

$$x = \frac{1}{2}\left(L + \frac{C_2}{c} + \frac{R}{rs} - \frac{R_0}{r} - \frac{sP}{c}\right)$$

(3) Answer the following questions for the problem (1) (Correct: +5 points, Wrong: -5 points, No answer: 0) for the minimization of the delay from the driver to the sink. Assume that $R_0 > \frac{R}{s}$ and $C_2 > sP$.

- If C_2 increases, x increases. (True / False)
- If c increases, x increases. (True / False)
- If R increases, x increases. (True / False)
- If r increases, x increases. (True / False)
- If R_0 increases, x increases. (True / False)
- If P increases, x increases. (True / False)