EE434

ASIC and Digital Systems

Midterm Exam 1

Feb. 25, 2022. (2:10pm – 3pm)

Instructor: Dae Hyun Kim

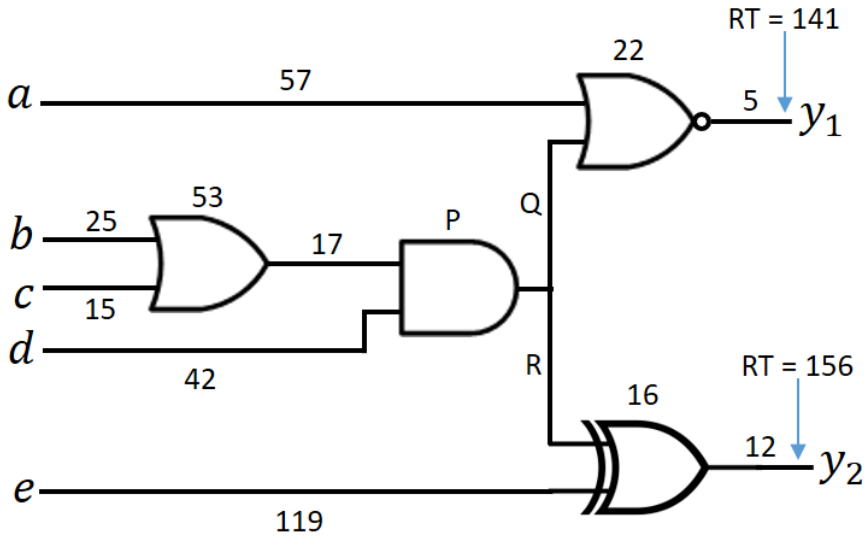
Name:

WSU ID:

Problem	Points	
1	20	
2	70	
3	60	
Total	150	

Problem #1 (20 points)

The following figure shows the delays (in ps) of the gates and nets of a logic design. The required times (RTs) at the output nodes are given as shown below. All the inputs have zero arrival time. $(P, Q, R > 0)$



1) Express the slack at the output y_1 using P and/or Q and/or R. (You can also use MIN, MAX operators.) (5 points)

$$AT = MAX(57, 95 + P + Q) + 27 = 122 + P + Q$$

$$Slack = RT - AT = 141 - (122 + P + Q) = 19 - P - Q$$

2) Express the slack at the output y_2 using P and/or Q and/or R. (You can also use MIN, MAX operators.) (5 points)

$$AT = MAX(95 + P + R, 119) + 28 = MAX(P + R, 24) + 123$$

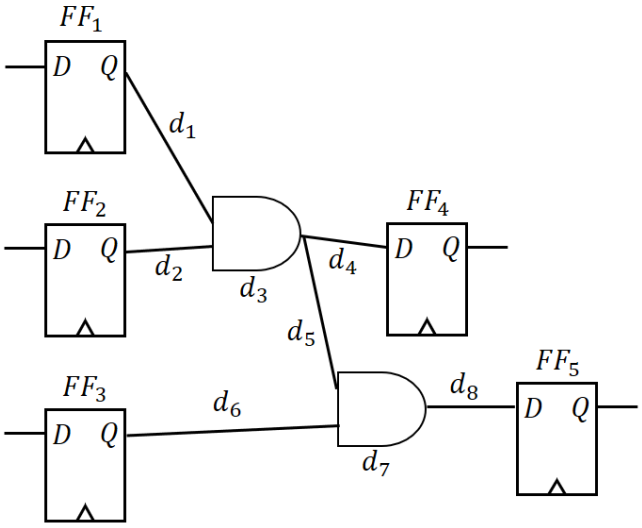
$$Slack = RT - AT = 128 - MAX(95 + P + R, 119) = 33 - MAX(P + R, 24)$$

3) Suppose P, Q, R are positive integers and satisfy $P + Q + R = 30$. Find P, Q, R that make the slacks at both y_1 and y_2 positive or zero. (Note: You can just find one set of (P, Q, R) because there are many (P, Q, R) sets satisfying the given condition.) (10 points)

$P + Q \leq 19$ and $P + R \leq 33$.

$$(P, Q, R) = (14,2,14)$$

Problem #2 (70 points)



- d_k: gate and net delays ($k = 1\sim8$)
- s_k: setup time of FF_k ($k = 1\sim5$)
- h_k: hold time of FF_k ($k = 1\sim5$)
- x_k: delay from the clock source to the clock pin of FF_k ($k = 1\sim5$)

- T_{CLK}: clock period
- MIN, MAX: MIN, MAX operators

(1) Show all the setup time inequalities in the design (10 points). (You can show all the inequalities without using the MIN, MAX operators, or show them using the MIN, MAX operators.)

$$MAX(x_1 + c_1 + d_1, x_2 + c_2 + d_2) + d_3 + d_4 \leq x_4 + T_{CLK} - s_4$$

$$MAX(MAX(x_1 + c_1 + d_1, x_2 + c_2 + d_2) + d_3 + d_5, x_3 + c_3 + d_6) + d_7 + d_8 \leq x_5 + T_{CLK} - s_5$$

(2) Show all the hold time inequalities in the design (10 points).

$$x_4 + h_4 \leq MIN(x_1 + c_1 + d_1, x_2 + c_2 + d_2) + d_3 + d_4$$

$$x_5 + h_5 \leq MIN(MIN(x_1 + c_1 + d_1, x_2 + c_2 + d_2) + d_3 + d_5, x_3 + c_3 + d_6) + d_7 + d_8$$

Notation: FFx-FFy is the path from the output of FFx to the input of FFy.

Answer the following questions. To fix a problem, you can increase or decrease the delay of only one net or gate (i.e., only one of $d_1 \sim d_8$). If there are multiple ways to fix a problem, you should choose the best one. If you cannot fix it, just say "cannot fix it" and explain why.

(3) $FF_2 - FF_4$ has a hold time violation. How would you fix it? (5 points)

Increase d_2.

(4) $FF_1 - FF_4$ and $FF_2 - FF_4$ have setup time violations. How would you fix both at the same time? (5 points)

Decrease d_4. (Decreasing d_3 might violate the hold time from FF_1 (or FF_2) to FF_5.)

(5) $FF_1 - FF_4$ and $FF_2 - FF_4$ have hold time violation. How would you fix both at the same time? (5 points)

Increase d_4. (Increasing d_3 might violate the setup time from FF_1 (or FF_2) to FF_5.)

(6) $FF_1 - FF_4$ and $FF_1 - FF_5$ have setup time violations. How would you fix both at the same time? (5 points)

Decrease d_1.

(7) $FF_1 - FF_4$ has a setup time violation and $FF_1 - FF_5$ has a hold time violation. How would you fix both at the same time? (5 points)

Cannot fix both at the same time. Can fix only one of them.

(8) $FF_1 - FF_4$ and $FF_2 - FF_5$ have setup time violations. How would you fix both at the same time? (5 points)

Decrease d_3.

(9) $FF_1 - FF_4$ has a hold time violation and $FF_2 - FF_5$ has a setup time violation. How would you fix both at the same time? (5 points)

Cannot fix both at the same time. Can fix only one of them.

(10) $FF_1 - FF_4$ has a setup time violation and $FF_2 - FF_5$ has a hold time violation. How would you fix both at the same time? (5 points)

Cannot fix both at the same time. Can fix only one of them.

(11) $FF_1 - FF_5$ and $FF_3 - FF_5$ have setup time violations. How would you fix both at the same time? (5 points)

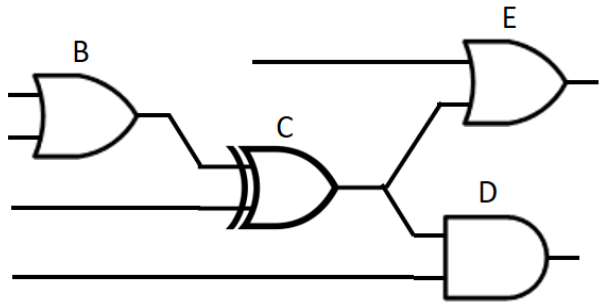
Decrease d_7 or d_8.

(12) $FF_1 - FF_5$ and $FF_2 - FF_5$ hold time violations and $FF_3 - FF_5$ has a setup time violation. How would you fix both at the same time? (5 points)

Cannot fix both at the same time.

Problem #3 (60 points)

The following shows three gates B, C, and D, which are in the middle of a circuit.



"A gate has a setup (or hold) time violation" means that at least one of the paths going through the gate violates given setup (or hold) time constraints.

Answer the following questions. Correct: +3 points, Wrong: -3 points, No answer: 0.

(1) It is possible that gate B has a setup-time violation and gate E has a setup-time violation too. (**True** / False)

(2) It is possible that gate B has a setup-time violation and gate E has a hold-time violation. (**True** / False)

(3) It is possible that gate B has a hold-time violation and gate E has a setup-time violation. (**True** / False)

(5) It is possible that gate B has a setup-time violation, but gate E does not have any setup-time violation. (**True** / False)

(6) It is possible that gate B has a setup-time violation, but gate E does not have any hold-time violation. (**True** / False)

(7) It is possible that gate B has a hold-time violation, but gate E does not have any setup-time violation. (**True** / False)

(8) It is possible that gate B has a hold-time violation, but gate E does not have any hold-time violation. (**True** / False)

(9) It is possible that gate D has a setup-time violation and gate E has a setup-time violation too. (**True** / False)

(10) It is possible that gate D has a setup-time violation and gate E has a hold-time violation. (**True** / False)

(11) It is possible that gate D has a hold-time violation and gate E has a setup-time violation. (**True** / False)

(12) It is possible that gate D has a hold-time violation and gate E has a hold-time violation too. (**True** / False)

(13) It is possible that gate D has a setup-time violation, but gate E does not have any setup-time violation. (**True** / False)

(14) It is possible that gate D has a setup-time violation, but gate E does not have any hold-time violation. (**True** / False)

(15) It is possible that gate D has a hold-time violation, but gate E does not have any setup-time violation. (**True** / False)

(16) It is possible that gate D has a hold-time violation, but gate E does not have any hold-time violation. (**True** / False)

(17) It is possible that gates B and D have setup-time violations, but gate C does not have any setup-time violation. (True / **False**)

(18) It is possible that gates B and D have setup-time violations, but gate C does not have any hold-time violation. (**True** / False)

(19) It is possible that gates B and D have hold-time violations, but gate C does not have any setup-time violation. (**True** / False)

(20) It is possible that gates B and D have hold-time violations, but gate C does not have any hold-time violation. (True / **False**)