EE434

ASIC and Digital Systems

Midterm Exam 2

Apr. 13, 2022. (2:10pm – 3pm)

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Name:

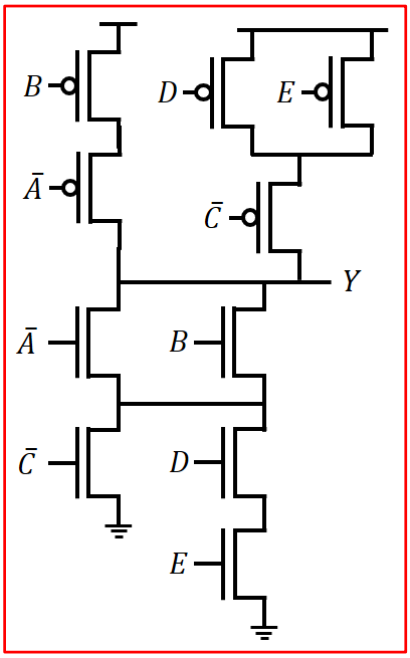
WSU ID:

Problem	Points	
1	10	
2	10	
3	10	
4	10	
5	10	
6	20	
7	20	
8	20	
9	10	
Total	120	

Problem #1 (Static CMOS, 10 points)

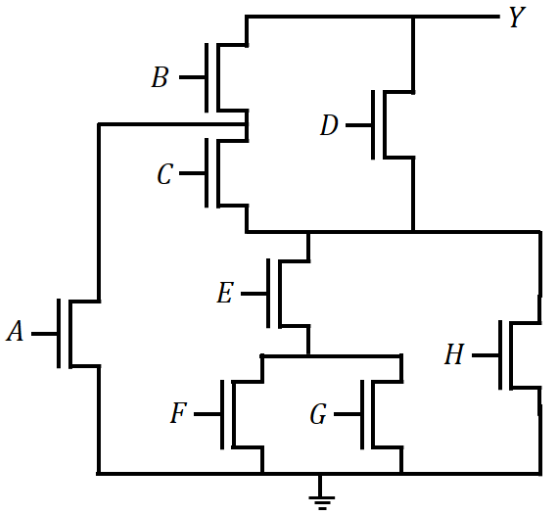
Design the following function (draw a transistor-level schematic) using the static CMOS logic design methodology. Available input: A, B, C, D, E. Try to minimize the # TRs.

$$Y = A \cdot \bar{B} + C \cdot (\bar{D} + \bar{E})$$



Problem #2 (Static CMOS, 10 points)

The following schematic shows the NFET network of a static CMOS logic gate.

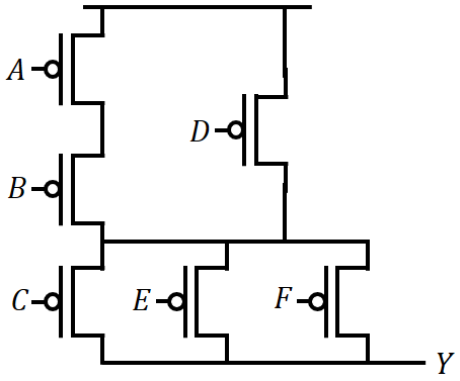


Express the output Y as a function of the input signals.

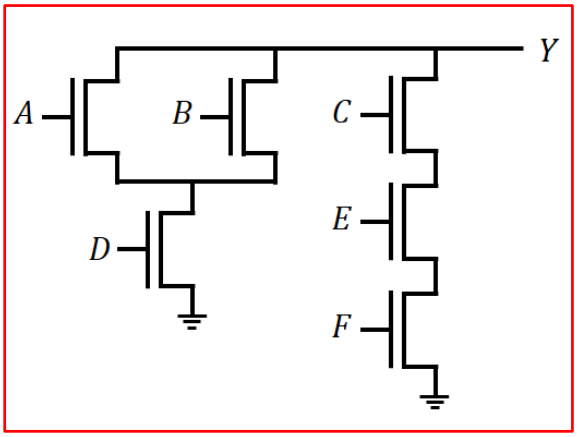
$$Y = \overline{A \cdot (B + C \cdot D) + (B \cdot C + D) \cdot \big(H + E \cdot (F + G)\big)}$$

Problem #3 (Static CMOS, 10 points)

The following schematic shows the PFET network of a static CMOS logic gate.



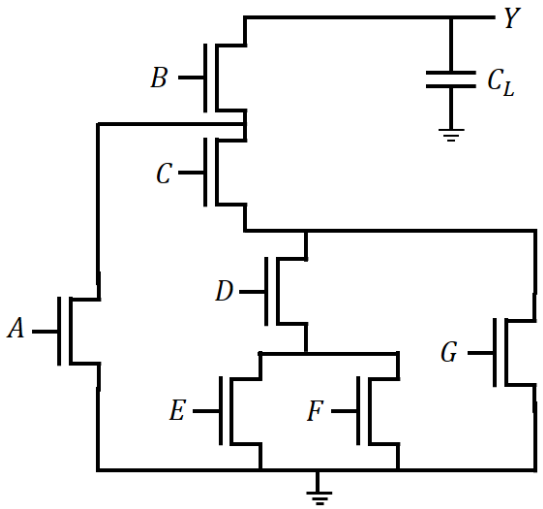
Design an NFET network for the logic gate.



Problem #4 (TR Sizing, 10 points)

$k = \frac{\mu_n}{\mu_p}$. R_n is the resistance of a 1X NFET (whose width is w_{min}). "$h \times$" for a TR means that the width of the TR is $h \cdot w_{min}$.

The following figure shows the NFET network of a static CMOS logic gate.



Size the transistors in the NFET network (show the size of each TR below). Timing constraint: $\tau_f \leq R_n C_L$ (τ_f is the fall delay). Try to minimize the total transistor width.

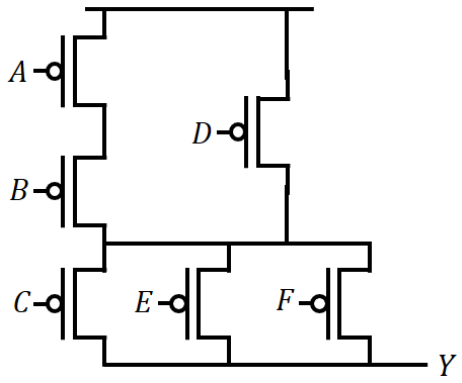
A: 4/3X B: 4X C: 4X D: 4X

E: 4X F: 4X G: 2X

Problem #5 (TR Sizing, 10 points)

$k = \frac{\mu_n}{\mu_p}$. R_n is the resistance of a 1X NFET (whose width is w_{min}). "$h\times$" for a TR means that the width of the TR is $h \cdot w_{min}$.

The following figure shows the PFET network of a static CMOS logic gate.



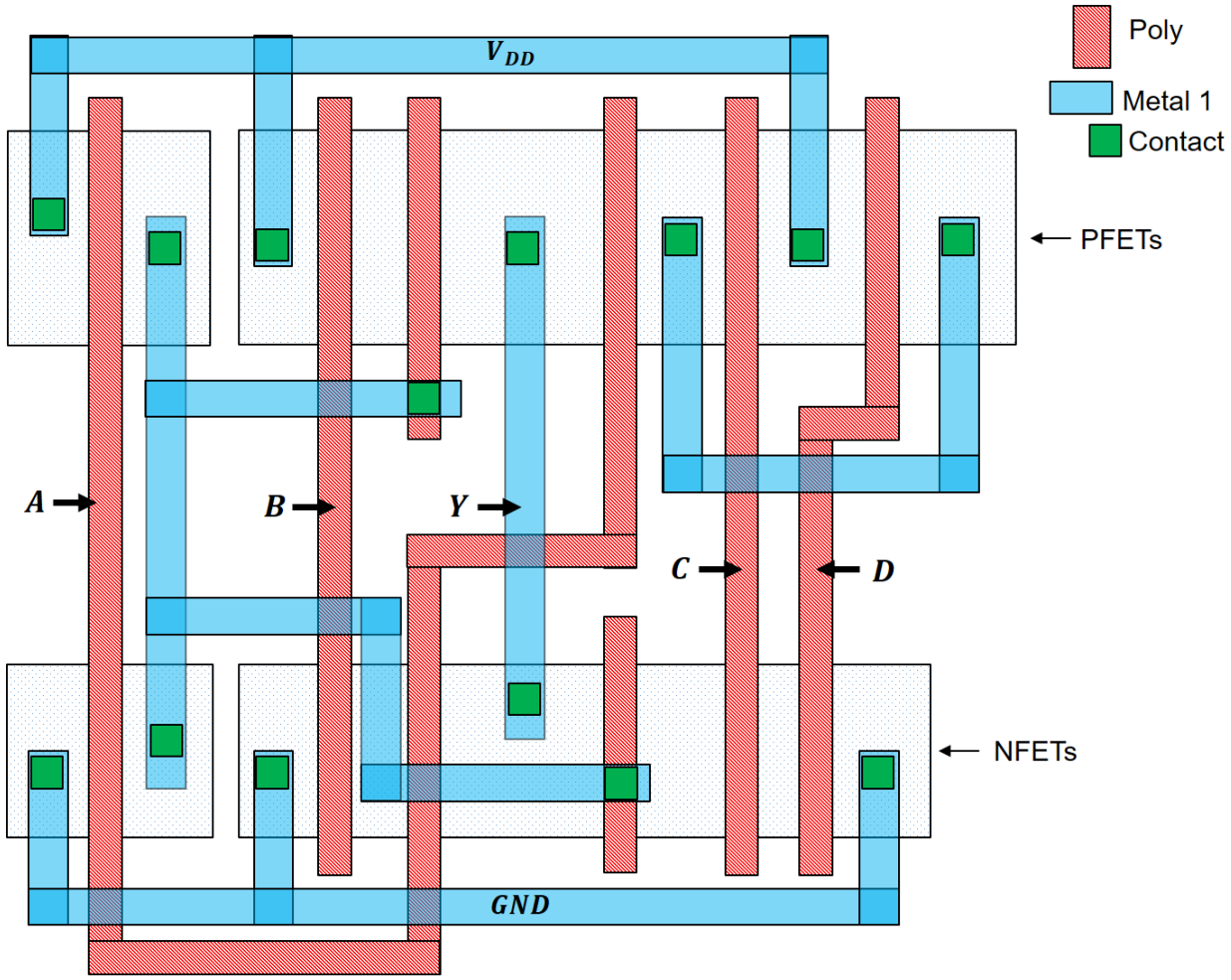
Size the transistors in the NFET network (show the size of each TR below). Timing constraint: $\tau_r \leq 0.25 R_n C_L$ (τ_r is the rise delay). Try to minimize the total transistor width.

A: 12kX B: 12kX C: 12kX

D: 6kX E: 12kX F: 12kX

Problem #6 (Layout, 20 points)

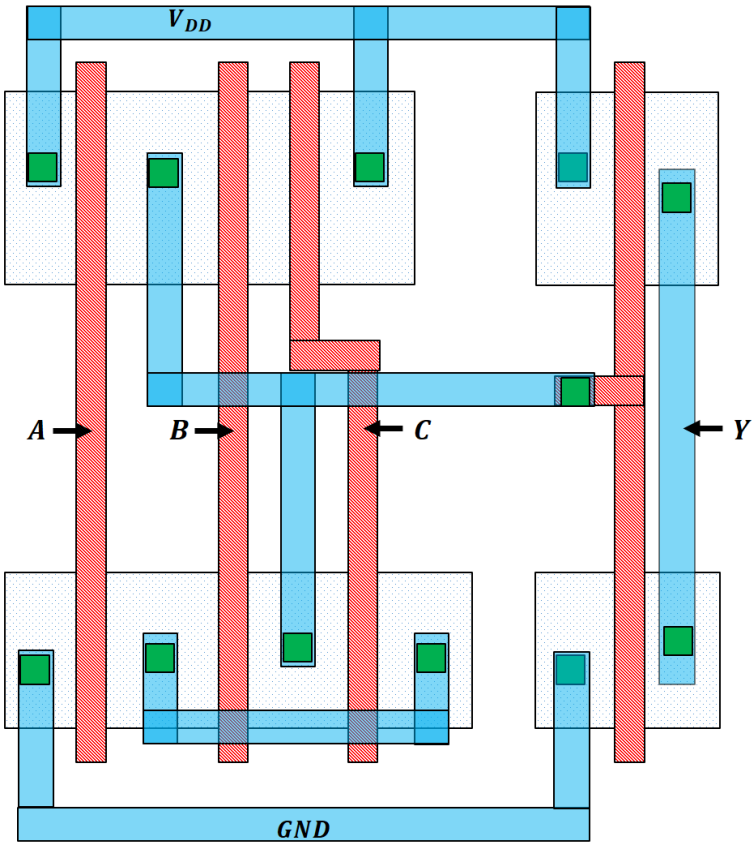
Express the output Y as a Boolean function of the input signals, A, B, C, and D.



$$Y = A \cdot \bar{B} + \bar{A} \cdot (\overline{C \cdot D})$$

Problem #7 (Layout, 20 points)

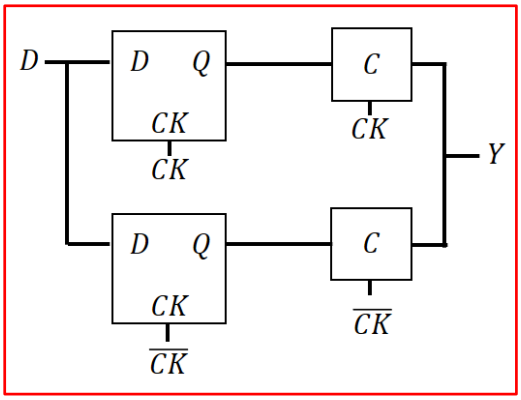
Draw a layout for $Y = A \cdot (B + C)$. (Use solid-line rectangles/polygons for Metal 1 wires, dotted rectangles/polygons for the poly (gate), and black-filled rectangles for contacts.)



Problem #8 (Logic Design, 20 points)

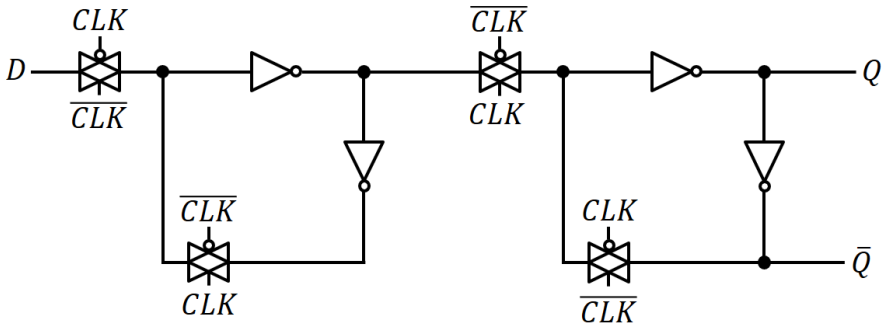
Design a dual-edge D flip flop (it captures the data input D whenever the clock signal goes high or low) using two single-edge D flip flops and some more gates (AND, NAND, NOR, ..., transmission gates, tristate inverters, tristate buffers, ...).

- Both of the two single-edge D flip flops could be positive-edge-triggered (PET) or negative-edge-triggered (NET), or one of them can be PET and the other can be NET.



Problem #9 (Logic Design, 10 points)

Modify the following D flip flop design so that you can add an “EN(ABLE)” signal.



- If EN is 1, the flip flop works as a D flip flop.
- If EN is 0, the flip flop output holds the current output value (i.e., it does not capture the input data D).

Replace D by $EN \cdot D + \overline{EN} \cdot Q$.