EE434

ASIC and Digital Systems

Final Exam

May 2, 2023. (1:30pm – 3:30pm)

Instructor: Dae Hyun Kim

Name:

WSU ID:

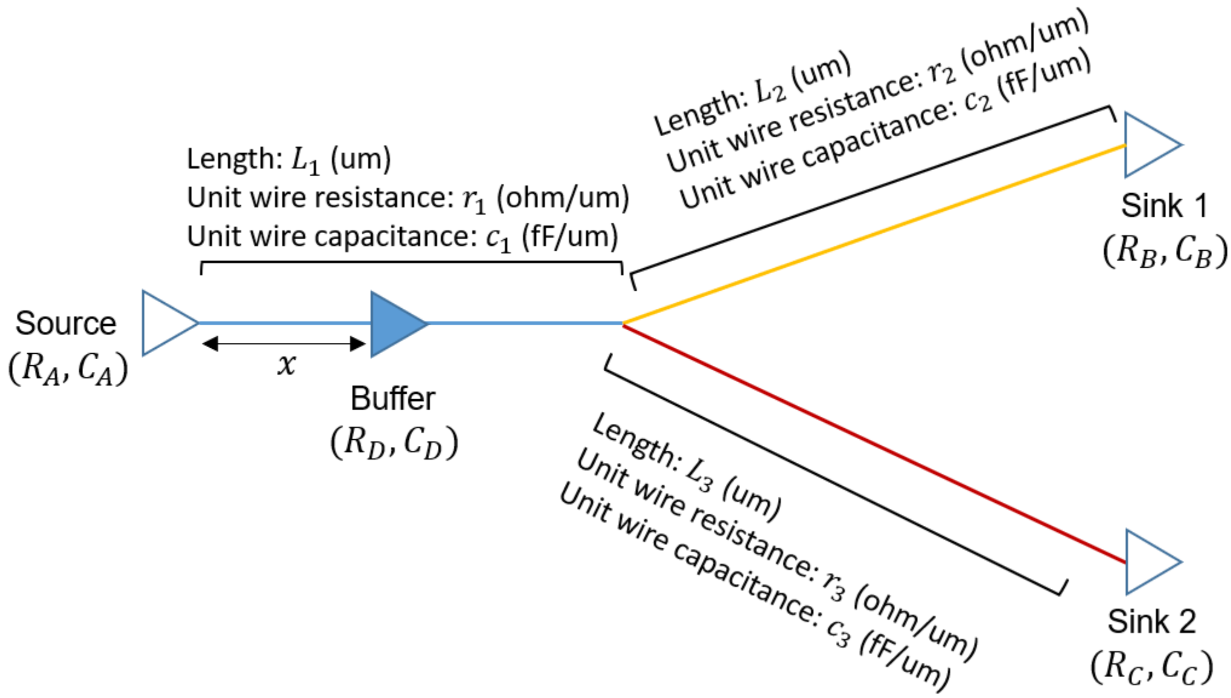
Problem	Points	
1	100	
2	90	
3	100	
4	90	
Total	380	

* Allowed: Books, cheat sheets, class notes, notebooks, calculators, watches, laptops, smartphones, tablet PCs, etc.

* Not allowed: Chatting apps, iMessage, etc. (basically, don't talk to anyone)

Problem #1 (Interconnect Optimization, 100 points)

The following figure shows a net optimized by a buffer.



Notice that (R, C) is the (output resistance, input capacitance) of the corresponding cell. x is the optimal location of the buffer ($0 < x < L_1$). We ignore the internal delay of the buffer. Use the PI model for each wire segment for delay estimation. We want to minimize the delay from the source to Sink 1 in this problem.

(1) Express the delay from the source to Sink 1 before the buffer insertion. (10 points)

$$d_{1,before} = r_2L_2\left(C_B + \frac{c_2L_2}{2}\right) + r_1L_1\left(C_B + C_C + c_2L_2 + c_3L_3 + \frac{c_1L_1}{2}\right) + R_A(C_B + C_C + c_1L_1 + c_2L_2 + c_3L_3)$$

(2) Express the delay from the source to Sink 1 after the buffer insertion. (10 points)

$$d_{1,after} = r_1x\left(C_D + \frac{c_1x}{2}\right) + R_A(C_D + c_1x) +$$

$$r_2L_2\left(C_B + \frac{c_2L_2}{2}\right) + r_1(L_1 - x)\left(C_B + C_C + c_2L_2 + c_3L_3 + \frac{c_1(L_1 - x)}{2}\right) + R_D(C_B + C_C + c_1(L_1 - x) + c_2L_2 + c_3L_3)$$

(3) Assuming the buffer insertion reduces the delay from the source to Sink 1, find the optimal location x of the buffer. (10 points)

$$\frac{dd_{1,after}}{dx} = r_1 C_D + r_1 c_1 x + R_A c_1 - r_1(C_B + C_C + c_2 L_2 + c_3 L_3) - r_1 c_1 (L_1 - x) - R_D c_1 = 0.$$

$$2 r_1 c_1 x = r_1(C_B + C_C + c_1 L_1 + c_2 L_2 + c_3 L_3) + R_D c_1 - (r_1 C_D + R_A c_1)$$

$$\therefore x = \frac{L_1}{2} + \frac{1}{2c_1}(C_B + C_C + c_2 L_2 + c_3 L_3) + \frac{R_D - R_A}{2r_1} - \frac{C_D}{2c_1}$$

(4) Answer the following questions. Correct: +5 points. Wrong: -5 points. Min: 0 points.

- If L_1 increases, then x increases too. (True / False)
- If L_2 increases, then x increases too. (True / False)
- If L_3 increases, then x increases too. (True / False)
- If R_A increases, then x increases too. (True / False)
- If R_D increases, then x increases too. (True / False)
- If C_B increases, then x increases too. (True / False)
- If C_C increases, then x increases too. (True / False)
- If C_D increases, then x increases too. (True / False)

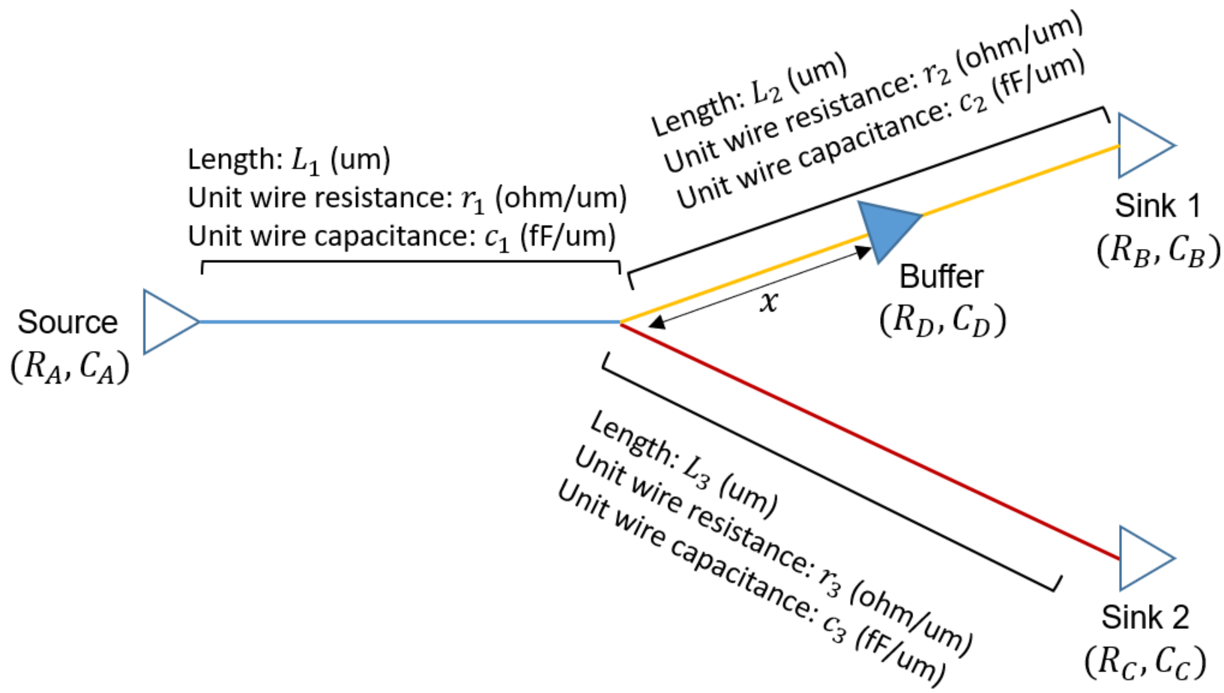
(5) Answer the following questions. Correct: +5 points. Wrong: -5 points. Min: 0 points.

Assume $R_D < R_A$. Assume C_D is negligible.

- If r_1 increases, then x increases too. (True / False)
- If r_2 increases, then x increases too. (True / False)
- If r_3 increases, then x increases too. (True / False)
- If c_1 increases, then x increases too. (True / False)
- If c_2 increases, then x increases too. (True / False)
- If c_3 increases, then x increases too. (True / False)

Problem #2 (Interconnect Optimization, 100 points)

The following figure shows a net optimized by a buffer.



Notice that (R, C) is the (output resistance, input capacitance) of the corresponding cell. x is the optimal location of the buffer ($0 < x < L_2$). We ignore the internal delay of the buffer. Use the PI model for each wire segment for delay estimation. We want to minimize the delay from the source to Sink 1 in this problem.

(1) Express the delay from the source to Sink 1 after the buffer insertion. (10 points)

$$d_{1,after} = r_2(L_2 - x)\left(C_B + \frac{c_2(L_2 - x)}{2}\right) + R_D\big(C_B + c_2(L_2 - x)\big) + r_2 x\left(C_D + \frac{c_2 x}{2}\right)$$
$$+ r_1 L_1\left(C_C + C_D + c_2 x + c_3 L_3 + \frac{c_1 L_1}{2}\right) + R_A(C_C + C_D + c_1 L_1 + c_2 x + c_3 L_3)$$

(2) Assuming the buffer insertion reduces the delay from the source to Sink 1, find the optimal location x of the buffer. (10 points)

$$\frac{dd_{1,after}}{dx} = -r_2 C_B - r_2 c_2(L_2 - x) - R_D c_2 + r_2 C_D + r_2 c_2 x + r_1 L_1 c_2 + R_A c_2 = 0.$$

$$2 r_2 c_2 x = r_2(C_B - C_D + c_2 L_2) + R_D c_2 - r_1 L_1 c_2 - R_A c_2$$

$$\therefore x = \frac{L_2}{2} + \frac{1}{2c_2}(C_B - C_D) + \frac{R_D - R_A}{2r_2} - \frac{r_1 L_1}{2r_2}$$

(3) Answer the following questions. Correct: +5 points. Wrong: -5 points. Min: 0 points.

- If L_1 increases, then x increases too. (True / False)
- If L_2 increases, then x increases too. (True / False)
- If R_A increases, then x increases too. (True / False)
- If R_D increases, then x increases too. (True / False)
- If C_B increases, then x increases too. (True / False)
- If C_D increases, then x increases too. (True / False)

(4) Answer the following questions. Correct: +10 points. Wrong: -10 points. Min: 0 points.

Notice that the optimal location x of the buffer found above (in Problem 2-2) is independent of L_3 and C_C (i.e., x does not have L_3 and C_C). In fact, however, the optimal location x is also dependent on L_3 and C_C. Answer the following questions NOT based on x you found above, BUT based on your intuition and knowledge considering the real-world factors.

- If L_3 increases, then x increases too. (True / False)
- If C_C increases, then x increases too. (True / False)

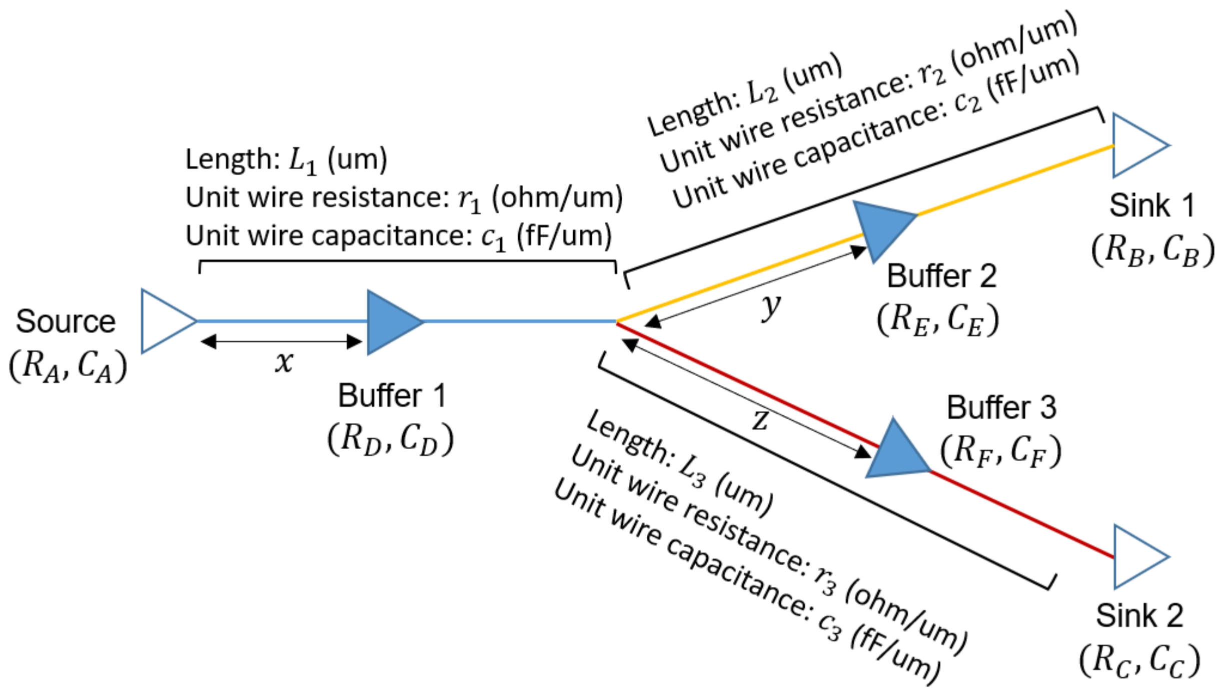
(5) Answer the following questions. Correct: +5 points. Wrong: -5 points. Min: 0 points.

Assume $R_D < R_A$. Assume C_D is negligible.

- If r_1 increases, then x increases too. (True / False)
- If r_2 increases, then x increases too. (True / False)
- If c_1 increases, then x increases too. (True / False)
- If c_2 increases, then x increases too. (True / False)

Problem #3 (Interconnect Optimization, 100 points)

The following figure shows a net optimized by three buffers.



Notice that (R, C) is the (output resistance, input capacitance) of the corresponding cell. x, y, z are the optimal locations of Buffer 1, 2, 3, respectively ($0 < x < L_1, 0 < y < L_2, 0 < z < L_3$). We ignore the internal delays of the buffers. We want to minimize both the delay from the source to Sink 1 and the delay from the source to Sink 2 in this problem.

Do not use the mathematical models we studied in the class. Instead, use your intuition to answer the following questions.

(1) Answer the following questions. Correct: +5 points. Wrong: -5 points. Min: 0 points.

- If L_1 increases, then x increases too. (True / False)
- If L_1 increases, then y increases too. (True / False)
- If L_2 increases, then x increases too. (True / False)
- If L_2 increases, then y increases too. (True / False)
- If L_2 increases, then z increases too. (True / False)

(2) Answer the following questions. Correct: +5 points. Wrong: -5 points. Min: 0 points.

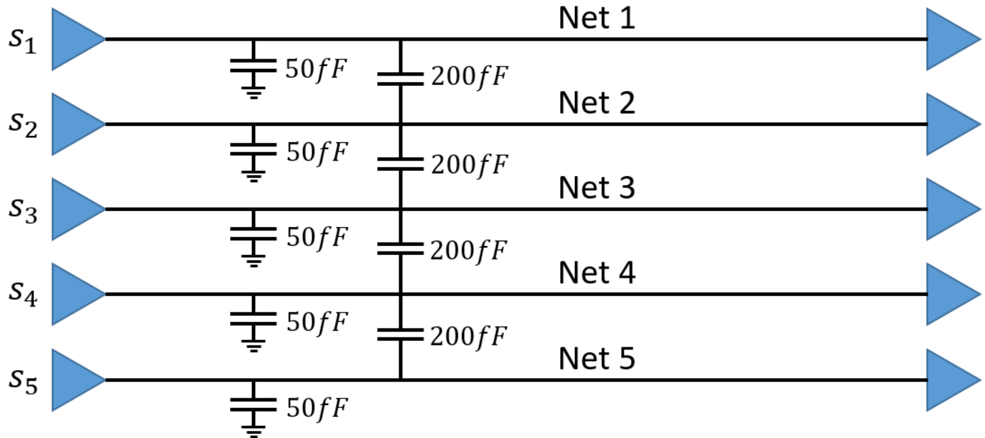
- If R_A increases, then x increases too. (True / False)
- If R_A increases, then y increases too. (True / False)
- If R_D increases, then x increases too. (True / False)
- If R_D increases, then y increases too. (True / False)

- If R_E increases, then x increases too. (True / False)
- If R_E increases, then y increases too. (True / False)
- If R_E increases, then z increases too. (True / False)

(3) Answer the following questions. Correct: +5 points. Wrong: -5 points. Min: 0 points.

- If C_D increases, then x increases too. (True / False)
- If C_D increases, then y increases too. (True / False)
- If C_E increases, then x increases too. (True / False)
- If C_E increases, then y increases too. (True / False)
- If C_E increases, then z increases too. (True / False)
- If C_B increases, then x increases too. (True / False)
- If C_B increases, then y increases too. (True / False)
- If C_B increases, then z increases too. (True / False)

Problem #4 (Coupling, 40 points)



This figure shows a bus composed of five nets. The following shows the data we are going to transfer through the bus:

$$0(initial) \rightarrow 5 \rightarrow 11 \rightarrow 4$$

We compute the power consumption for a signal transition as follows:

$$P = C_{t,eff} {V_{DD}}^2$$

where $V_{DD} = 1V$ and $C_{t,eff}$ is the sum of the effective capacitances.

(1) Compute the power consumption of the data transfer (three transitions) using the conventional 5-bit binary codes for the data. (20 points)

$$00000 \rightarrow 00101 \rightarrow 01011 \rightarrow 00100$$

- $00000 \rightarrow 00101$: $C = (50 + 200 + 200) + (50 + 200) = 700fF$
- $00101 \rightarrow 01011$: $C = (50 + 200 + 400) + (50 + 400 + 400) + (50 + 400) = 1950fF$
- $00101 \rightarrow 00100$: $C = (50 + 200 + 400) + (50 + 400 + 400) + (50 + 400) + (50) = 2000fF$

Thus, $P = 4650fW = 4.65pW$

(2) Compute the power consumption of the data transfer using the 5-bit forbidden pattern free crosstalk avoidance code. Ignore the power consumption of the encoder/decoder. (20 points)

$$00000 \rightarrow 01100 \rightarrow 11110 \rightarrow 00111$$

- $00000 \rightarrow 01100$: $C = (50 + 200) + (50 + 200) = 500fF$
- $01100 \rightarrow 11110$: $C = (50 + 200) + (50 + 200 + 200) = 700fF$
- $11110 \rightarrow 00111$: $C = (50) + (50 + 200) + (50 + 200) = 550fF$

Thus, $P = 1750fW = 1.75pW$

(3) Let's estimate the efficiency of the forbidden pattern free crosstalk avoidance code (FPF-CAC). (50 points)

- The Fibonacci sequence is defined as follows:
  - $f_1 = 1$
  - $f_2 = 1$
  - $f_{k+2} = f_{k+1} + f_k$
- Complete the following. (10 points)
  - $f_3 = 2$
  - $f_4 = 3$
  - $f_5 = 5$
  - $f_6 = 8$
  - $f_7 = 13$
  - $f_8 = 21$
  - $f_9 = 34$
  - $f_{10} = 55$
  - $f_{11} = 89$
  - $f_{12} = 144$
  - $f_{13} = 233$
  - $f_{14} = 377$
- In page 33 of the interconnect lecture note, the # bits we need to represent a number in FPF-CAC is determined by the "MSB stage". For a given data (number) v, we should find the max. f_{m+1} satisfying $v \geq f_{m+1}$. For example, if $v = 19$, $f_1 \leq \cdots \leq f_7 \leq 19 < f_8$, so the max. f_{m+1} satisfying the above condition is f_7. Thus, $m + 1 = 7$, so $m = 6$, so we need 6 bits to represent 19 in FPF-CAC.
- The max. data (number) that an m-bit FPF-CAC code can represent is as follows (Complete the following from $m = 7$ to 12) (20 points):
  - $m = 1$: 1
  - $m = 2$: 2
  - $m = 3$: 4
  - $m = 4$: 7
  - $m = 5$: 12
  - $m = 6$: 20
  - $m = 7$: 33
  - $m = 8$: 54
  - $m = 9$: 88
  - $m = 10$: 143
  - $m = 11$: 232
  - $m = 12$: 376
- Similarly, the max. data (number) that an m-bit conventional binary code (e.g., $20 = 10100_2$) can represent is as follows (Complete the following from $m = 7$ to 12) (10 points):
  - $m = 1$: 1
  - $m = 2$: 3

- $m = 3$: 7
- $m = 4$: 15
- $m = 5$: 31
- $m = 6$: 63
- $m = 7$: 127
- $m = 8$: 255
- $m = 9$: 511
- $m = 10$: 1023
- $m = 11$: 2047
- $m = 12$: 4095

- Thus, the efficiency is estimated as follows (Complete the following from $m = 7$ to 12) (10 points):
  - $m = 1$: 1/1 = 1.0
  - $m = 2$: 2/3 = 0.67
  - $m = 3$: 4/7 = 0.57
  - $m = 4$: 7/15 = 0.47
  - $m = 5$: 12/31 = 0.39
  - $m = 6$: 20/63 = 0.32
  - $m = 7$: 33/127 = 0.26
  - $m = 8$: 54/255 = 0.21
  - $m = 9$: 88/511 = 0.17
  - $m = 10$: 143/1023 = 0.14
  - $m = 11$: 232/2047 = 0.11
  - $m = 12$: 376/4095 = 0.09