EE434

ASIC and Digital Systems

Midterm Exam 1

Mar. 1, 2023. (2:10pm – 3pm)

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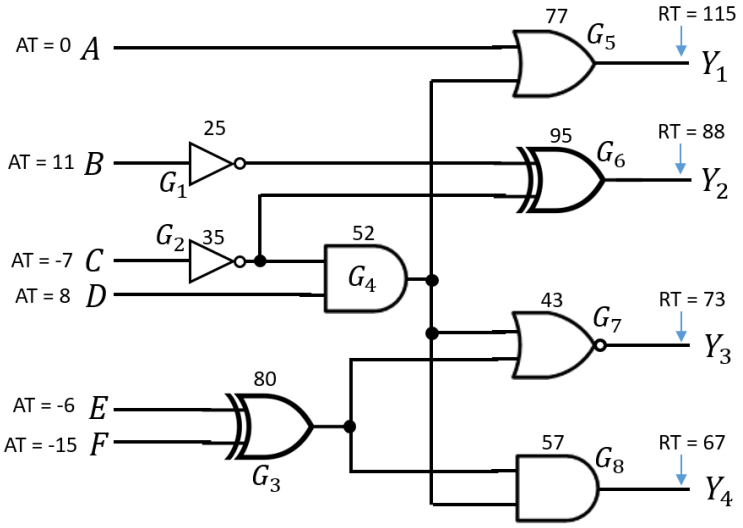
Name:

WSU ID:

Problem	Points	
1	20	
2	50	
3	90	
Total	160	

Problem #1 (20 points)

The following figure shows the delays of the gates of a logic design. All the nets have zero delay. Required times (RTs) at the output nodes and Arrival times (ATs) at the input nodes are given as shown below.



(1) (5 points) Express the slack at the output Y_1.

$$AT = MAX(0 + 77, -7 + 35 + 52 + 77, 8 + 52 + 77) = 157$$

$$Slack = RT - AT = 115 - 157 = -42$$

(2) (5 points) Express the slack at the output Y_3.

$$AT = MAX(-7 + 35 + 52 + 43, 8 + 52 + 43, -6 + 80 + 43, -15 + 80 + 43) = 123$$

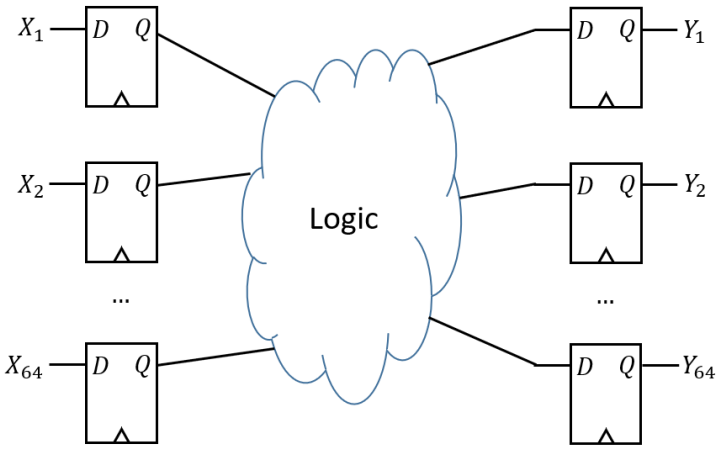
$$Slack = RT - AT = 73 - 123 = -50$$

(3) (10 points) If the delay of G_2 goes down by 5, does the slack of the path from D to Y_3 go up? If no, just say no. If yes, calculate the increment of the slack.

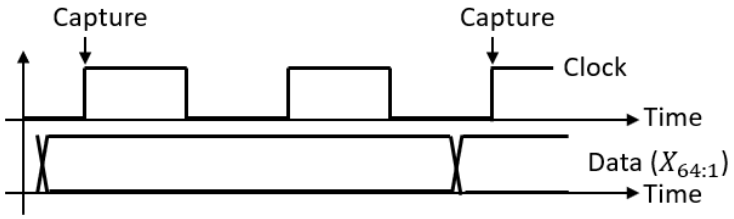
The slack of D-Y_3 is RT-AT where RT=73 and AT is the sum of the delays of G4 and G7. Thus, it is not affected by the delay of G2. The answer is NO.

Problem #2 (50 points)

The following figure shows a two-cycle pipeline stage. “Two-cycle” means capturing occurs every two cycles.



The following figure shows two waveforms of the clock and data.



- L_{i-k}: the logic delay from input X_i to output Y_k (e.g., L_{64-2} means the logic delay from input X_{64} to output Y_2)
- s: setup time of a flip-flop
- h: hold time of a flip-flop
- x: delay from the clock source to the clock pin of a flip-flop
- c: clk-to-Q delay of a flip-flop
- T_{CLK}: clock period
- MIN, MAX: MIN, MAX operators

(1) Show all the setup time inequalities of the design (10 points). (Use the MIN, MAX operators.)

$$x + c + MAX(L_{1-1}, \dots, L_{64-64}) \leq x + 2 \cdot T_{CLK} - s$$

(2) Show all the hold time inequalities of the design (10 points). (Use the MIN, MAX operators.)

$$x + h \leq x + c + MIN(L_{1-1}, \ldots, L_{64-64})$$

Answer the following questions for the figure above. Correct: +5 points, Wrong: -5 points, No answer: 0. Min: 0 points.

(3) Assume WNS < 0 and TNS < 0. In this case, if s goes up, WNS goes down. (**True** / False)

(4) Assume WNS < 0 and TNS < 0. In this case, if s goes up, TNS goes down. (**True** / False)

(5) Assume WNS < 0 and TNS < 0. In this case, if c goes up, WNS goes down. (**True** / False)

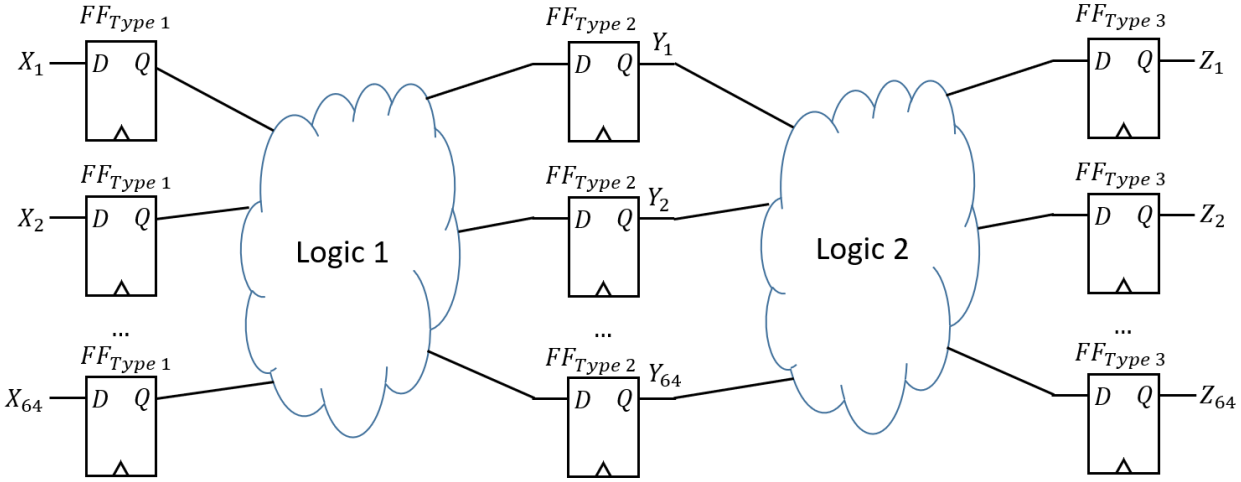
(6) Assume WNS < 0 and TNS < 0. In this case, if c goes up, TNS goes down. (**True** / False)

(7) Assume WNS < 0 and TNS < 0. In this case, if x goes up, WNS goes down. (True / **False**)

(8) Assume WNS < 0 and TNS < 0. In this case, if x goes up, TNS goes down. (True / **False**)

Problem #3 (90 points)

The following shows two pipeline stages of a system.



- L_{i-k}: the logic delay from X_i to Y_k (e.g., L_{64-2} means the logic delay from X_{64} to Y_2)
- M_{i-k}: the logic delay from Y_i to Z_k (e.g., M_{8-16} means the logic delay from Y_8 to Z_{16})
- s_k: setup time of a flip-flop of type k
- h_k: hold time of a flip-flop of type k
- x_k: delay from the clock source to the clock pin of a flip-flop of type k
- c_k: clk-to-Q delay of a flip-flop of type k

Answer the following questions. Correct: +5 points, Wrong: -5 points, No answer: 0. Min: 0 points. WNS and TNS are obtained for the whole system (including both the first and second pipeline stages.)

(1) Assume WNS < 0 and TNS < 0. In this case, if s_2 goes up, WNS goes down. (True / **False**)

(2) Assume WNS < 0 and TNS < 0. In this case, if s_2 goes up, TNS goes down. (True / **False**)

(3) Assume WNS < 0 and TNS < 0. In this case, if s_3 goes up, WNS goes down. (True / **False**)

(4) Assume WNS < 0 and TNS < 0. In this case, if s_3 goes up, TNS goes down. (True / **False**)

(5) Assume WNS < 0 and TNS < 0. In this case, if x_2 goes up, WNS goes down. (True / **False**)

(6) Assume WNS < 0 and TNS < 0. In this case, if x_2 goes up, TNS goes down. (True / **False**)

(7) Assume WNS < 0 and TNS < 0. In this case, if x_3 goes up, WNS goes down. (True / **False**)

(8) Assume WNS < 0 and TNS < 0. In this case, if x_3 goes up, TNS goes down. (True / **False**)

(9) Assume WNS < 0 and TNS < 0. In this case, if c_2 goes up, WNS goes down. (True / **False**)

(10) Assume WNS < 0 and TNS < 0. In this case, if c_2 goes up, TNS goes down. (True / **False**)

(11) Assume WNS < 0 and TNS < 0. In this case, if c_3 goes up, WNS goes down. (True / **False**)

(12) Assume WNS < 0 and TNS < 0. In this case, if c_3 goes up, TNS goes down. (True / False)

(13) Assume WNS < 0 and TNS < 0. In this case, if both s_2 and s_3 go up, WNS goes down. (**True** / False)

(14) Assume WNS < 0 and TNS < 0. In this case, if both s_2 and s_3 go up, TNS goes down. (**True** / False)

(15) Assume WNS < 0 and TNS < 0. In this case, if both x_2 and x_3 go up, WNS goes down. (True / **False**)

(16) Assume WNS < 0 and TNS < 0. In this case, if both x_2 and x_3 go up, TNS goes down. (True / **False**)

(17) Assume WNS < 0 and TNS < 0. In this case, if both c_2 and c_3 go up, WNS goes down. (True / **False**)

(18) Assume WNS < 0 and TNS < 0. In this case, if both c_2 and c_3 go up, TNS goes down. (True / **False**)

(19) Assume WNS < 0 and TNS < 0. In this case, if both s_1 and s_2 go up, WNS goes down. (True / **False**)

(20) Assume WNS < 0 and TNS < 0. In this case, if both s_1 and s_2 go up, TNS goes down. (True / **False**)

(21) Assume WNS < 0 and TNS < 0. In this case, if both x_1 and x_2 go up, WNS goes down. (True / **False**)

(22) Assume WNS < 0 and TNS < 0. In this case, if both x_1 and x_2 go up, TNS goes down. (True / **False**)

(23) Assume WNS < 0 and TNS < 0. In this case, if both c_1 and c_2 go up, WNS goes down. (**True** / False)

(24) Assume WNS < 0 and TNS < 0. In this case, if both c_1 and c_2 go up, TNS goes down. (**True** / False)

(25) Assume WNS < 0 and TNS < 0. In this case, if s_1, s_2, and s_3 go up, WNS goes down. (**True** / False)

(26) Assume WNS < 0 and TNS < 0. In this case, if s_1, s_2, and s_3 go up, TNS goes down. (**True** / False)

(27) Assume WNS < 0 and TNS < 0. In this case, if x_1, x_2, and x_3 go up, WNS goes down. (True / **False**)

(28) Assume WNS < 0 and TNS < 0. In this case, if x_1, x_2, and x_3 go up, TNS goes down. (True / **False**)

(29) Assume WNS < 0 and TNS < 0. In this case, if c_1, c_2, and c_3 go up, WNS goes down. (**True** / False)

(30) Assume WNS < 0 and TNS < 0. In this case, if c_1, c_2, and c_3 go up, TNS goes down. (**True** / False)