EE434

ASIC and Digital Systems

Midterm Exam 2

Apr. 7, 2023. (2:10pm – 3pm)

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Name:

WSU ID:

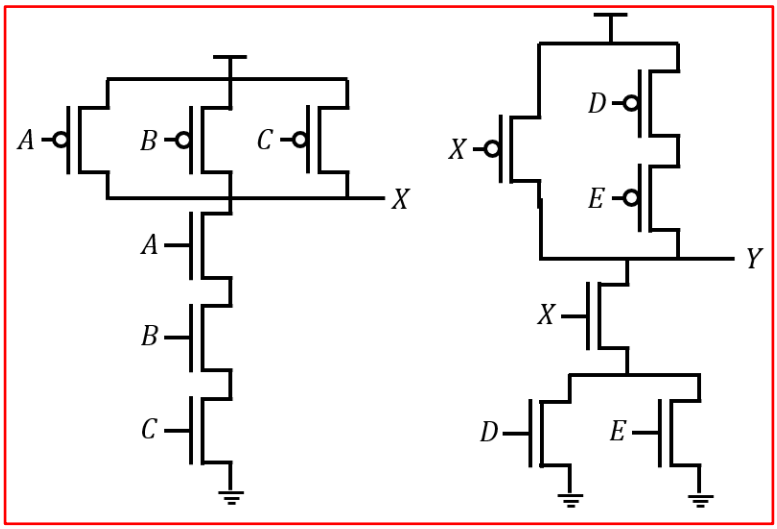
Problem	Points	
1	10	
2	10	
3	10	
4	10	
5	20	
6	20	
7	10	
Total	90	

Problem #1 (Static CMOS, 10 points)

Design the following function (draw a transistor-level schematic) using the static CMOS logic design methodology. Available input: A, B, C, D, E. Try to minimize the # TRs.

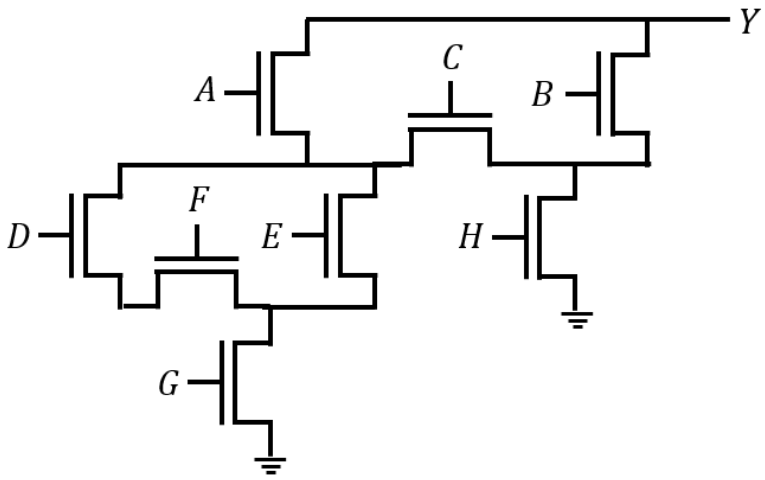
$$Y = A \cdot B \cdot C + \overline{D} \cdot \overline{E}$$

$$Y = \overline{\overline{A \cdot B \cdot C + \overline{D} \cdot \overline{E}}} = \overline{\overline{A \cdot B \cdot C} \cdot (D + E)}$$



Problem #2 (Static CMOS, 10 points)

The following schematic shows the NFET network of a static CMOS logic gate.

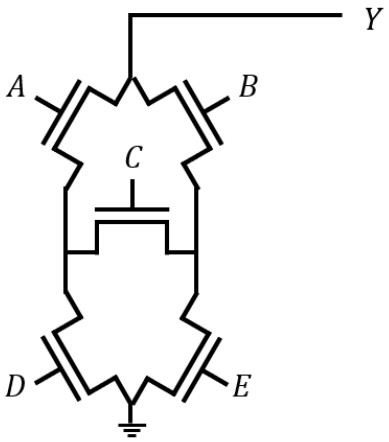


Express the output Y as a function of the input signals.

$$Y = \overline{A(CH + (DF + E)G) + B(H + C(DF + E)G)}$$

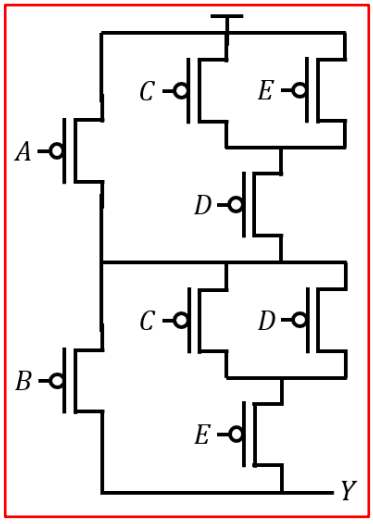
Problem #3 (Static CMOS, 10 points)

The following schematic shows the NFET network of a static CMOS logic gate.



Design a PFET network for the logic gate. Try to minimize # TRs.

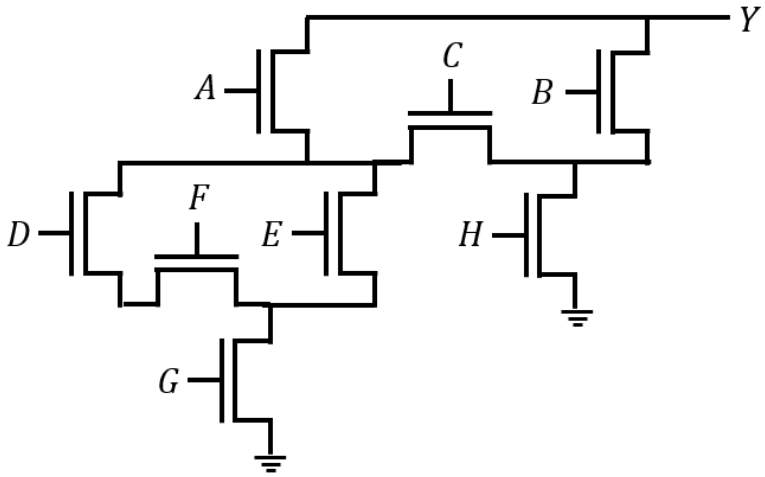
$$Y = \overline{A(D + CE) + B(E + CD)}$$



Problem #4 (TR Sizing, 10 points)

$k = \frac{\mu_n}{\mu_p}$. R_n is the resistance of a 1X NFET (whose width is w_{min}). "$h \times$" for a TR means that the width of the TR is $h \cdot w_{min}$.

The following figure shows the NFET network of a static CMOS logic gate.



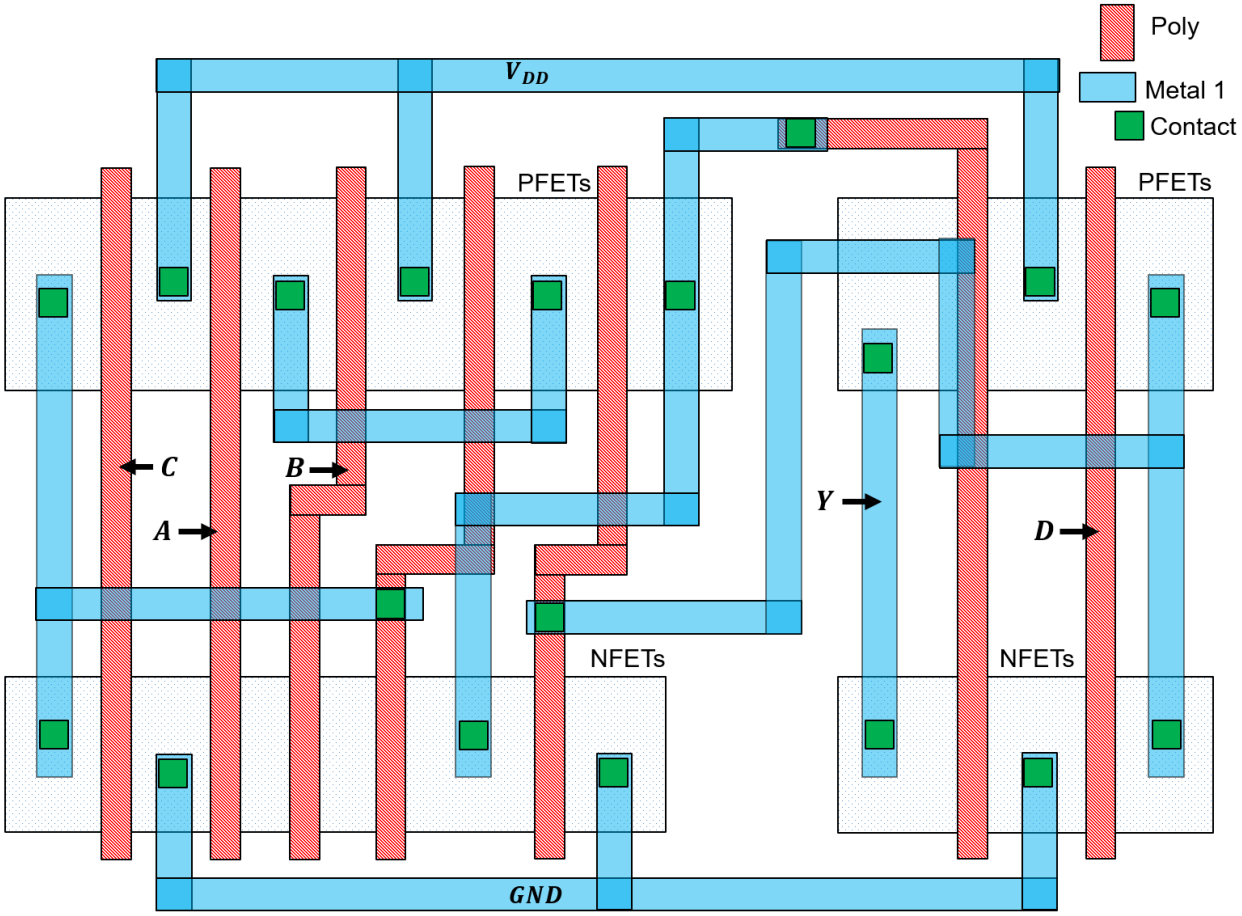
Size the transistors in the NFET network (show the size of each TR below). Timing constraint: $\tau_f \leq R_n C_L$ (τ_f is the worst-case fall delay). Try to minimize the total transistor width.

A: 2.5X B: 5X C: 5X D: 5X

E: 2.5X F: 5X G: 5X H: 2.5X

Problem #5 (Layout, 20 points)

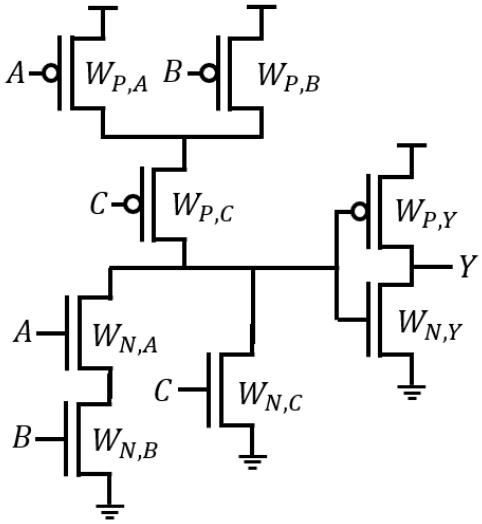
Express the output Y as a Boolean function of the input signals, A, B, C, and D.



$$Y = AB\bar{C} + \bar{D}$$

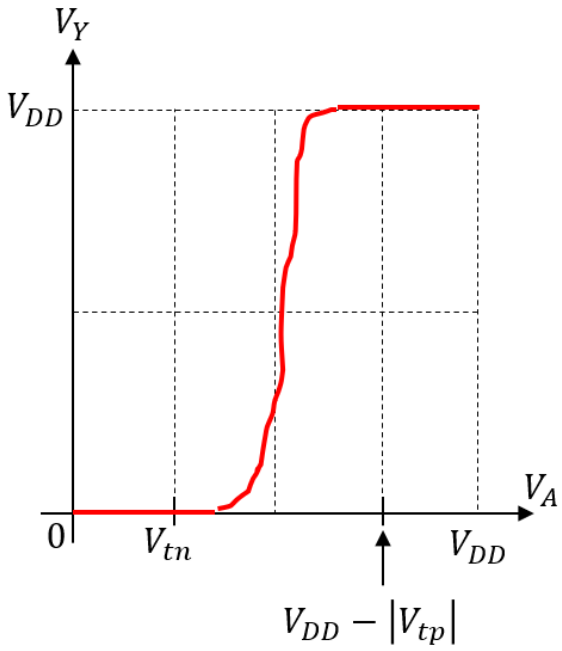
Problem #6 (DC Analysis, 20 points)

The following shows a design of $Y = A \cdot B + C$.



W_X is the width of the transistor X. Assume that the transistors have some proper widths.

(1) Draw its DC characteristic curve for $B = 1, C = 0$, and A switches from 0 to 1. Just a rough sketch will be accepted. (10 points)

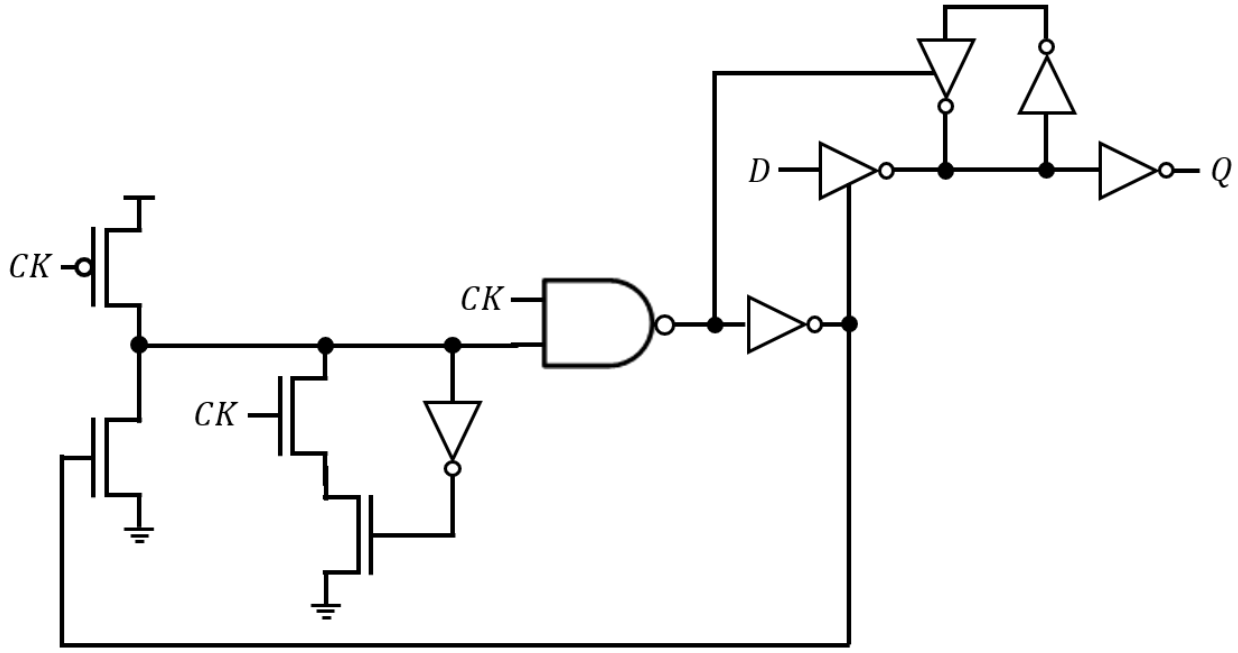


(2) Answer the following questions. Correct: +2 points, Wrong: -2 points, No answer: 0. Min: 0 points.

- If $W_{N,A}$ goes up, then the DC curve is shifted upward always at $V_A = \frac{V_{DD}}{2}$. (True / False)
- If $W_{N,C}$ goes up, then the DC curve is shifted upward always at $V_A = \frac{V_{DD}}{2}$. (True / False)
- If $W_{P,A}$ goes up, then the DC curve is shifted downward always at $V_A = \frac{V_{DD}}{2}$. (True / False)
- If $W_{P,C}$ goes up, then the DC curve is shifted downward always at $V_A = \frac{V_{DD}}{2}$. (True / False)
- If $W_{N,Y}$ goes up, then the DC curve is shifted upward always at $V_A = \frac{V_{DD}}{2}$. (True / False)

Problem #7 (Sequential Logic, 10 points)

What does the following circuit do? Describe its functionality in as much detail as possible. (D: data input. CK: clock. Q: data output)



Positive-edge-triggered D FF