EE434

ASIC and Digital Systems

Final Exam

May 1, 2024. (1:30pm – 3:30pm)

Instructor: Dae Hyun Kim

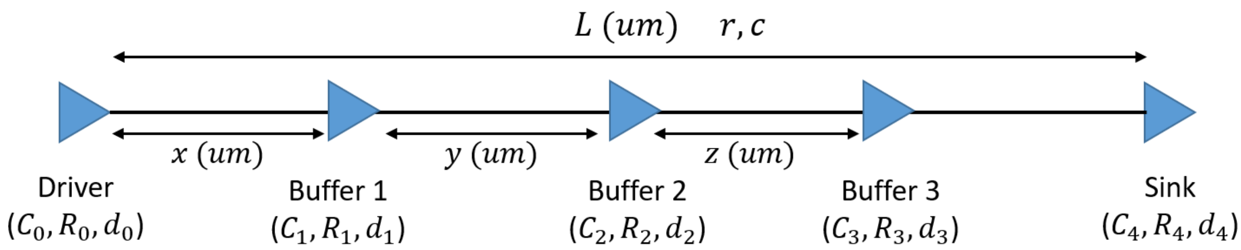
Name:

WSU ID:

Problem	Points	
1	100	
2	50	
3	50	
4	30	
5	40	
6	120	
Total	390	

Problem #1 (Interconnect Optimization, 100 points)

The following figure shows a net optimized by three buffers.



(A, B, C) of a cell denotes its (input cap., output resistance, internal delay). We ignore all the output capacitances of the cells. r and c are unit wire resistance and capacitance, respectively. L is the length from the Driver to the Sink.

- Given (constants): $C_0 - C_4, R_0 - R_4, d_0 - d_4, r, c, L$

Use the PI model for each wire segment for delay estimation. We want to find optimal x, y, z minimizing the delay from the output of the Driver to the input of the Sink.

(1) Express the delay from the output of the Driver to the input of the Sink after the buffer insertion. (20 points)

$\tau = R_0 \cdot (cx + C_1) + rxC_1 + \frac{1}{2}rcx^2 + d_1 + R_1 \cdot (cy + C_2) + ryC_2 + \frac{1}{2}rcy^2 + d_2 + R_2 \cdot (cz + C_3) + rzC_3 + \frac{1}{2}rcz^2 + d_3 + R_3 \cdot (cw + C_4) + rwC_4 + \frac{1}{2}rcw^2$ (where $w = L - (x + y + z)$)

(2) Find the optimal locations x, y, z that minimize the delay. (20 points)

$$\frac{\partial \tau}{\partial x} = R_0 c + rC_1 + rcx - R_3 c - rC_4 - rcw = 0.$$

$$\frac{\partial \tau}{\partial y} = R_1 c + rC_2 + rcy - R_3 c - rC_4 - rcw = 0.$$

$$\frac{\partial \tau}{\partial z} = R_2 c + rC_3 + rcz - R_3 c - rC_4 - rcw = 0.$$

$$x = \frac{L}{4} + \frac{1}{4r}\{(R_1 + R_2 + R_3) - 3R_0\} + \frac{1}{4c}\{(C_2 + C_3 + C_4) - 3C_1\}$$

$$y = \frac{L}{4} + \frac{1}{4r}\{(R_0 + R_2 + R_3) - 3R_1\} + \frac{1}{4c}\{(C_1 + C_3 + C_4) - 3C_2\}$$

$$z = \frac{L}{4} + \frac{1}{4r}\{(R_0 + R_1 + R_3) - 3R_2\} + \frac{1}{4c}\{(C_1 + C_2 + C_4) - 3C_3\}$$

$$w = \frac{L}{4} + \frac{1}{4r}\{(R_0 + R_1 + R_2) - 3R_3\} + \frac{1}{4c}\{(C_1 + C_2 + C_3) - 3C_4\}$$

(3) Answer the following questions. Correct: +4 points. Wrong: -4 points. Min: 0 points.

- If L increases, then x increases. (True / False)
- If L increases, then z increases. (True / False)

(4) Answer the following questions. Correct: +4 points. Wrong: -4 points. Min: 0 points.

- If R_0 increases, then z increases. (True / False)
- If R_1 increases, then x increases. (True / False)
- If R_1 increases, then y increases. (True / False)
- If R_1 increases, then z increases. (True / False)

(5) Answer the following questions. Correct: +4 points. Wrong: -4 points. Min: 0 points.

- If R_2 increases, then x increases. (True / False)
- If R_2 increases, then y increases. (True / False)
- If R_2 increases, then z increases. (True / False)

(6) Answer the following questions. Correct: +4 points. Wrong: -4 points. Min: 0 points.

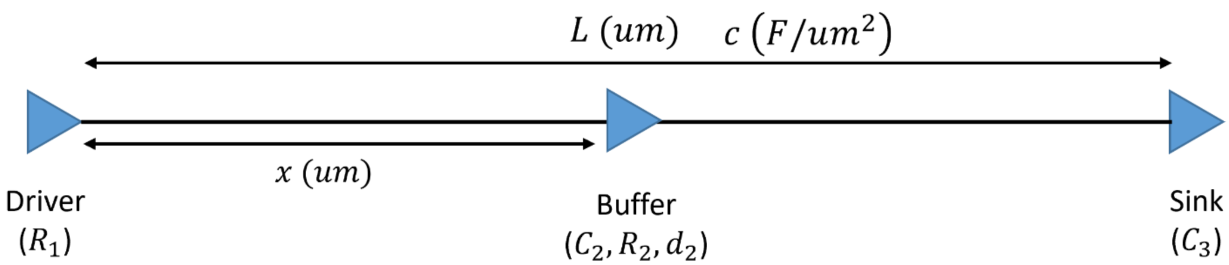
- If C_2 increases, then x increases. (True / False)
- If C_2 increases, then y increases. (True / False)
- If C_2 increases, then z increases. (True / False)

(7) Answer the following questions. Correct: +4 points. Wrong: -4 points. Min: 0 points.

- If C_3 increases, then x increases. (True / False)
- If C_3 increases, then y increases. (True / False)
- If C_3 increases, then z increases. (True / False)

Problem #2 (Interconnect Optimization, 50 points)

The following figure shows a net optimized by a buffer.



The output resistances of the driver and the buffer are R_1 and R_2, respectively. The input capacitances of the buffer and the sink are C_2 and C_3, respectively. d_2 is the internal delay of the buffer.

A new interconnect technology is used for the nets. The nets have no resistance ($r = 0$). However, the wire capacitance is proportional to the square of its length. In other words, the capacitance of a net of length $k(um)$ is ck^2.

Use the PI model for each wire segment for delay estimation. We want to minimize the delay from the output of the Driver to the input of the Sink.

(1) Express the delay from the output of the Driver to the input of the Sink after the buffer insertion. (10 points)

$$\tau = R_1 \cdot (cx^2 + C_2) + d_2 + R_2 \cdot (c(L-x)^2 + C_3)$$

(2) Find the optimal location x of the buffer that minimizes the delay. (10 points)

$$\frac{d\tau}{dx} = 2R_1cx - 2R_2c(L-x) = 0.$$

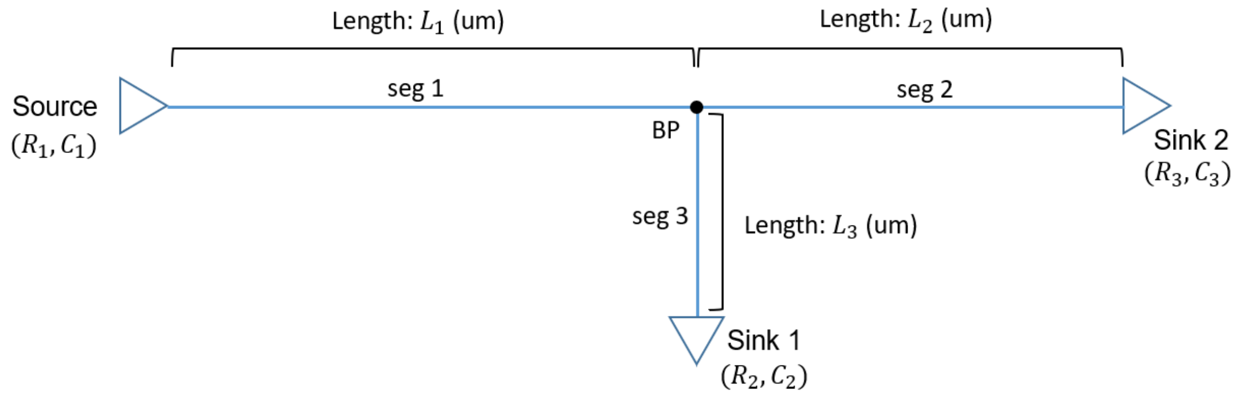
$$x = \frac{R_2L}{R_1 + R_2} = \frac{L}{1 + \frac{R_1}{R_2}}$$

(3) Answer the following questions. Correct: +5 points. Wrong: -5 points. Min: 0 points.

- If L increases, then x increases. (True / False)
- If R_1 increases, then x increases. (True / False)
- If R_2 increases, then x increases. (True / False)
- If C_2 increases, then x increases. (True / False)
- If C_3 increases, then x increases. (True / False)
- If c increases, then x increases. (True / False)

Problem #3 (Interconnect Optimization, 60 points)

The following figure shows a net having two sinks.



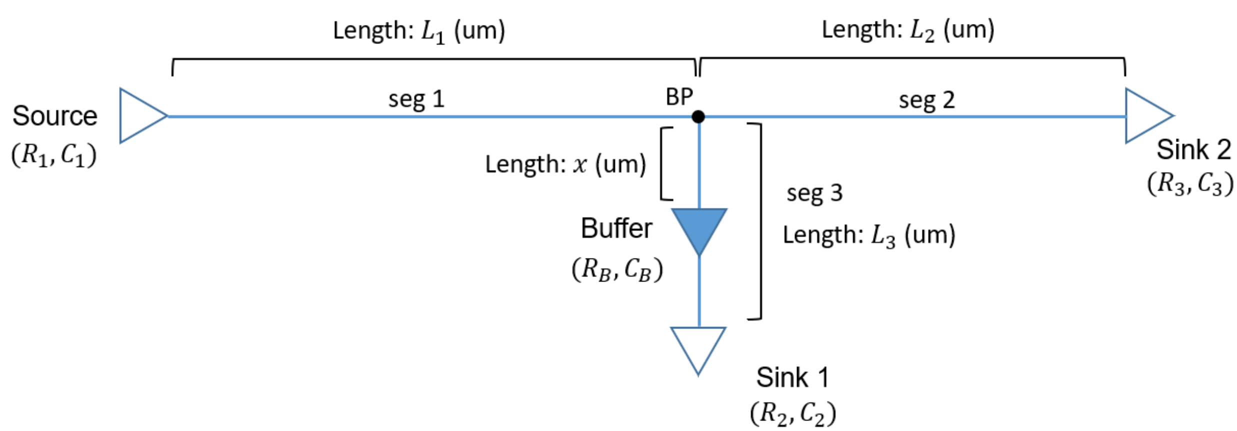
All the nets have the same unit wire resistance (r) and capacitance (c). (A,B) denotes (output resistance, input capacitance). We ignore output capacitance values.

<u>We are going to minimize the delay from the output of the source to the input of the sink 2.</u>

(1) Express the delay from the output of the source to the input of the sink 2. (10 points)

$$\tau = rL_2\left(\frac{1}{2}cL_2 + C_3\right) + rL_1\left(\frac{1}{2}cL_1 + cL_2 + cL_3 + C_2 + C_3\right) + R_1(cL_1 + cL_2 + cL_3 + C_2 + C_3)$$

Now, let's insert a buffer into the net. The output resistance and the input capacitance of the buffer is (R_B, C_B). Due to some restrictions, we insert the buffer into segment 3 as follows.



(2) Express the delay from the output of the source to the input of the sink 2 after the buffer insertion. (10 points)

$$\tau = rL_2\left(\frac{1}{2}cL_2 + C_3\right) + rL_1\left(\frac{1}{2}cL_1 + cL_2 + cx + C_B + C_3\right) + R_1(cL_1 + cL_2 + cx + C_B + C_3)$$

(3) Assume the range of x is $0 \leq x \leq L_3$. We insert the buffer into the location

- right after the branch point (BP) if $x = 0$.
- right before Sink 1 if $x = L_3$
- between BP and Sink 1 if $0 < x < L_3$.

Find the optimal location of the buffer. (10 points)

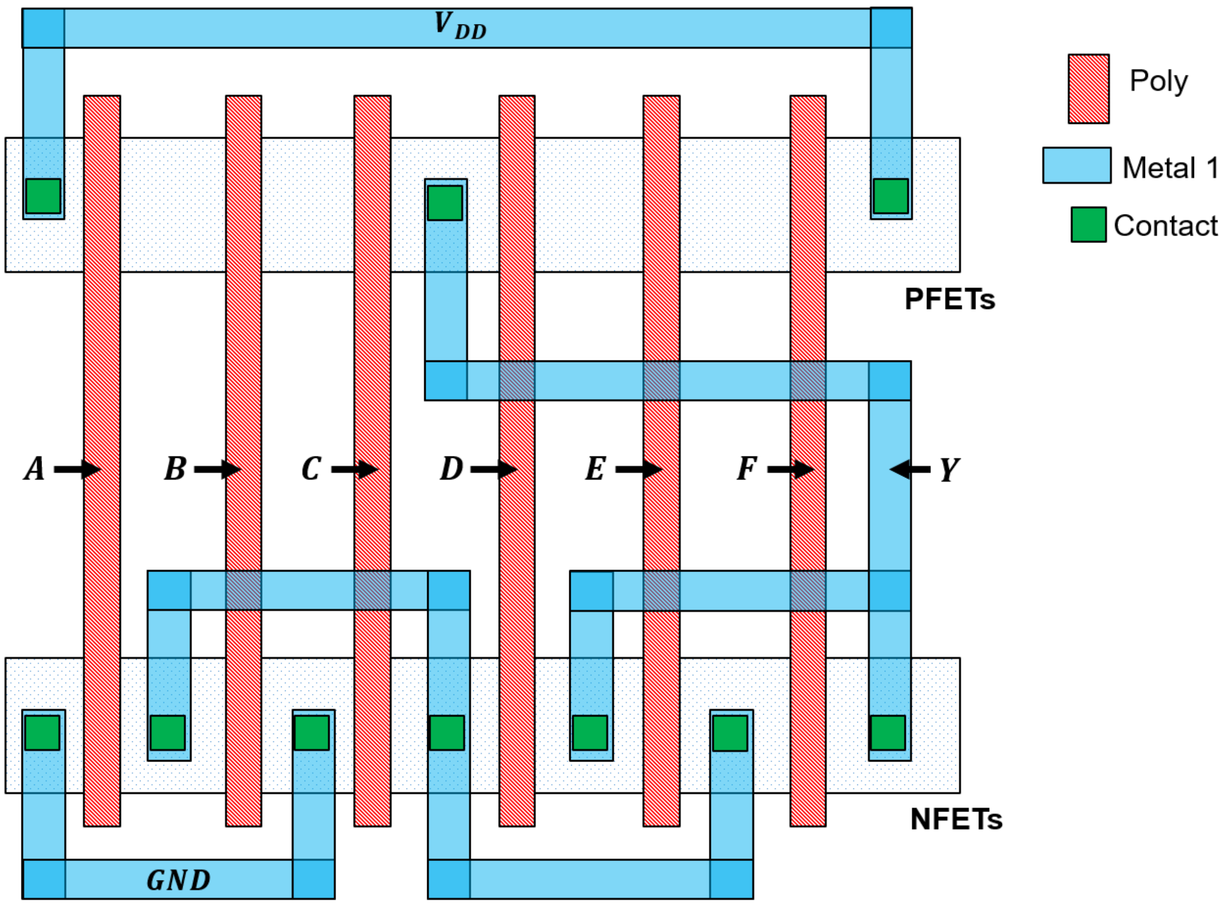
Since τ is an increasing function of x, $x = 0$ is the optimal location of the buffer.

(4) Answer the following questions. Correct: +5 points. Wrong: -5 points. Min: 0 points.

- If L_1 increases, then x increases. (True / False)
- If L_2 increases, then x increases. (True / False)
- If L_3 increases, then x increases. (True / False)
- If C_3 increases, then x increases. (True / False)

Problem #4 (Layout, 30 points)

Express the output Y as a Boolean function of the input signals, A, B, C, D, E, F.



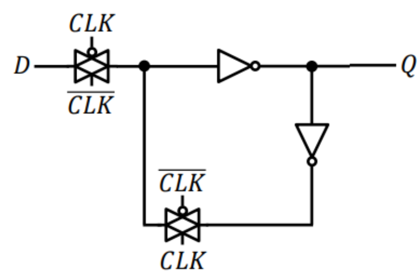
(1) Draw a transistor-level schematic for the layout. (20 points)

(2) Express Y as a function of the input signals. (10 points)

$$Y = \overline{(A + B + C) \cdot (D + E + F)}$$

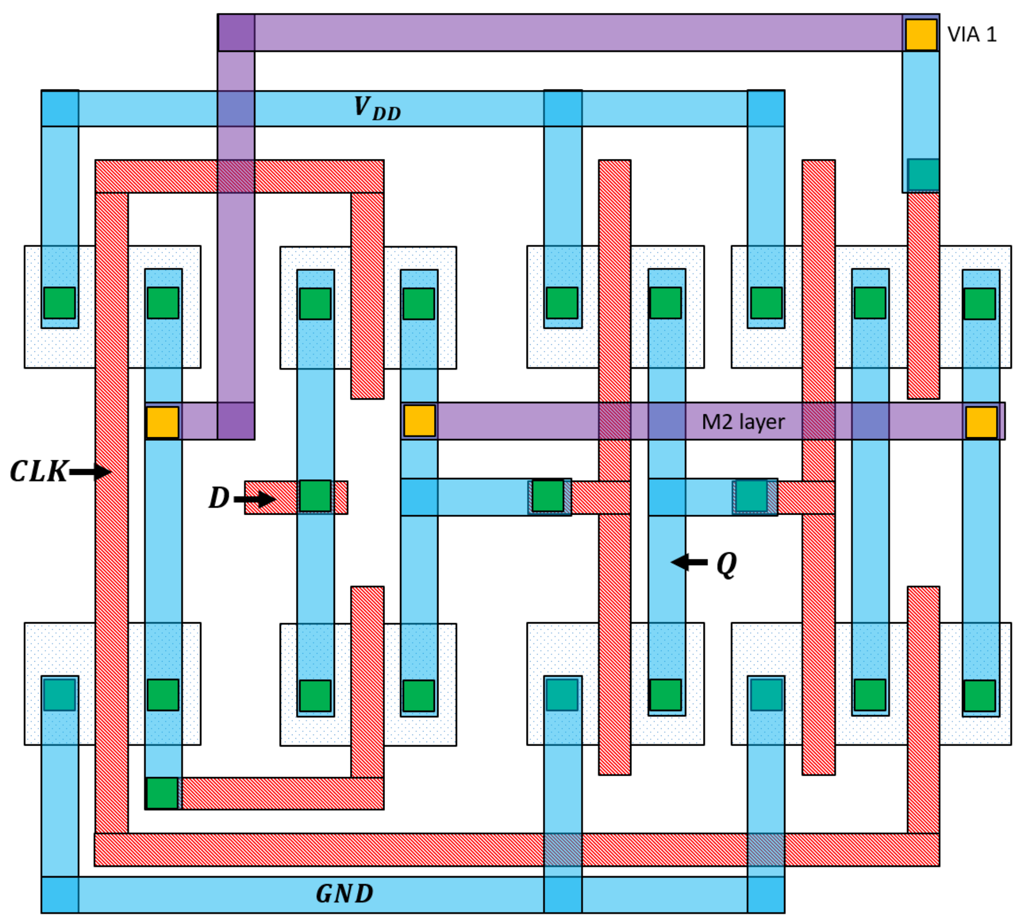
Problem #5 (Layout, 40 points)

Draw a layout for the following schematic. (It's a D-latch)

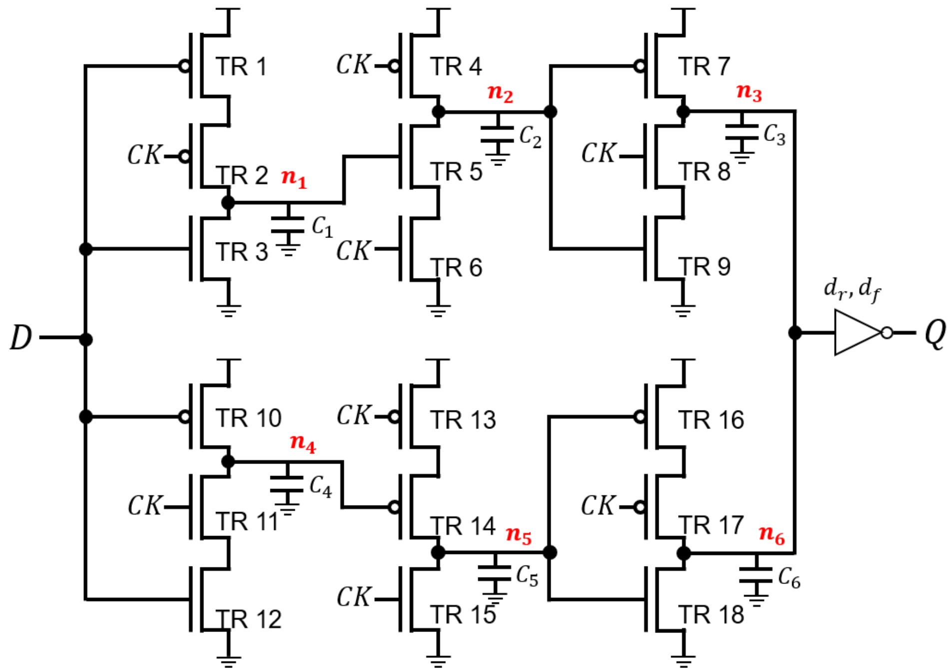


- Given input: D, CLK
- Output: Q

You can draw a simplified layout like the one shown in Problem #4. You don't need to show body contacts, n-well, p-well, etc. Use M1 and M2 layers for the metal layers.



Problem #6 (Flip Flops, 120 points)



The schematic above is a dual-edge D-FF design.

- The resistance of the PFET (or NFET) of TR # is $R_{p,\#}$ (or $R_{n,\#}$). For example, the resistance of the PFET of TR 16 is $R_{p,16}$. The resistance of the NFET of TR 18 is $R_{n,18}$.
- The rise and fall delays of the inverter are d_r and d_f, respectively.
- If an internal node becomes floating, you can assume that it holds its previous value. (i.e., we ignore all the leakage current.)
- If an internal node is not connected to a capacitor, you can ignore its parasitic capacitance.

(1) Find the clock-to-Q delay for D=0 and CK=0→1. This means that the DFF captures the value of D=0 when the clock goes high (0→1) and you are supposed to find the clock-to-Q delay in this case. (20 points)

D=0 and CK=0, so $n_1 = 1$, $n_2 = 1$, n_3 holds its current value. When CK goes high, TR6 is turned on, so it discharges n_2 (delay = $(R_{n,5} + R_{n,6})C_2$). Then, TR7 is turned on, and charges n_3 (delay = $R_{p,7}C_3$). Then, Q becomes 0 (delay = d_f).

Answer: $(R_{n,5} + R_{n,6})C_2 + R_{p,7}C_3 + d_f$.

(2) Find the clock-to-Q delay for D=1 and CK=0→1. (20 points)

D=1 and CK=0, so $n_1 = 0$, $n_2 = 1$, and n_3 holds its current value. When CK goes high, TR8 is turned on, so it discharges n_3 (delay = $(R_{n,8} + R_{n,9})C_3$). Then, Q becomes 1 (delay = d_r).

Answer: $(R_{n,8} + R_{n,9})C_3 + d_r$.

(3) Find the setup time for D=0 and CK=0→1. (20 points)

D=1 and CK=0, so $n_1 = 0$, $n_2 = 1$, and n_3 holds its current value.

When CK goes high, Q should become 0 (because we will capture D=0), so n_3 must be 1, then n_2 must be 0 after CK goes high. ($n_2 = 1$ before CK goes high because TR4 will charge n_2 when CK=0). This means TR 5 must be turned on, so $n_1 = 1$ before CK goes high. If D=1, then TR3 is on, so $n_1 = 0$. Now, if D switches to 0, then n_1 is charged to 1, which must be done before CK goes high.

Thus, the setup time is $(R_{p,1} + R_{p,2})C_1$.

(4) Find the setup time for D=1 and CK=0→1. (20 points)

When CK goes high, Q should become 1, so n_3 must be 0, then n_2 must be 1. When CK is 0, n_2 is charged to 1, so TR5 should be turned off before CK goes high. Thus, n_1 must be 0 before CK goes high. If D goes high, then TR3 is turned on and n_1 is discharged.

Thus, the setup time is $R_{n,3}C_1$.

(5) Find the hold time for D=0 and CK=0→1. (20 points)

If D=0 and CK=0, then $n_1 = 1$, $n_2 = 1$, and n_3 holds its current value.

Now, CK goes high, so n_2 becomes 0, n_3 goes high, and Q goes low.

Suppose D switches to 1 soon after CK goes high, but before n_2 goes low. Then, n_1 becomes 0, so n_2 wouldn't be 0. Thus, this is wrong.

Suppose D switches to 1 after CK goes high and n_2 goes low, but n_3 goes high. Since $n_2 = 0$, even if D is 1 and n_1 becomes 0, n_2 will hold its current value (0), which will charge n_3, which will lead Q to 0.

Thus, the hold time is $(R_{n,5} + R_{n,6})C_2$.

(6) Find the hold time for D=1 and CK=0→1. (20 points)

If D=1 and CK=0, then $n_1 = 0$, $n_2 = 1$, and n_3 holds its current value.

Now, CK goes high, so n_2 is still 1 and n_3 goes low, and Q becomes 1.

Suppose D switches to 0 soon after CK goes high. Then, n_1 is still 0, so it doesn't affect the downstream.

Thus, the hold time is almost zero.