EE466

VLSI System Design

Midterm Exam

Dec. 14, 2020. (4pm – 6pm)

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Name:

WSU ID:

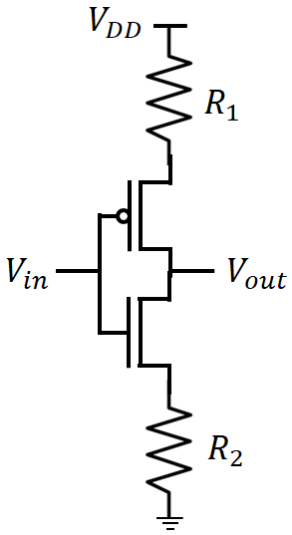
Problem	Points	
1	10	
2	10	
3	20	
4	10	
5	15	
6	10	
7	25	
8	25	
9	20	
Total	145	

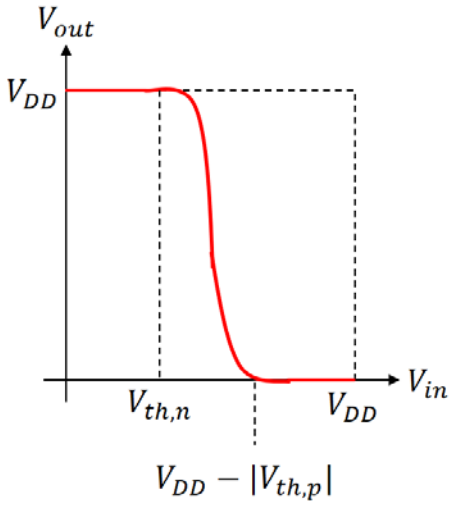
* Allowed: Textbooks, cheat sheets, class notes, notebooks, calculators, watches

* Not allowed: Electronic devices (smart phones, tablet PCs, laptops, etc.) except calculators and watches

Problem #1 (DC Analysis, 10 points)

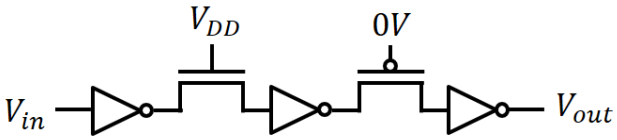
Draw a DC curve (V_{in} vs. V_{out}) for the following logic circuit. You should also show some important data points on the curve.

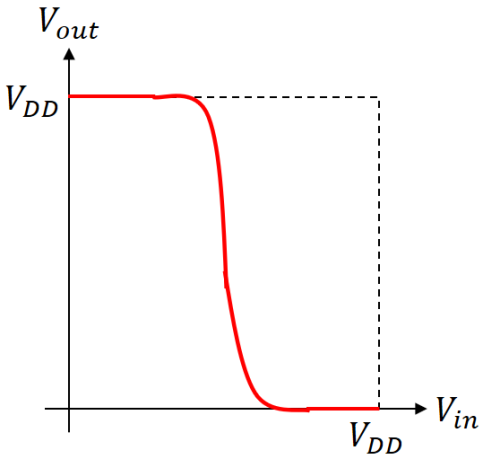




Problem #2 (DC Analysis, 10 points)

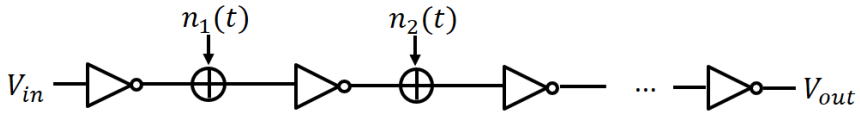
Draw a DC curve (V_{in} vs. V_{out}) for the following logic circuit. Assume $V_{th,n} = |V_{th,p}|$ for all the NFETs and PFETs. Just a rough sketch will be accepted.

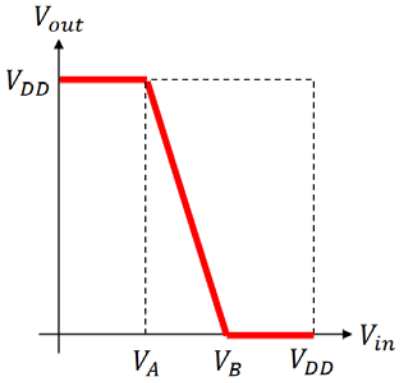




Problem #3 (Noise, 20 points)

The following shows a chain of inverters. $n_i(t)$ is a noise source and added to the signal as shown below. The range of $n_i(t)$ is $[-\frac{V_{DD}}{8}, \frac{V_{DD}}{4}]$. All the inverters have the same DC characteristics shown below. V_{in} is 0V for logic 0 and V_{DD} for logic 1. Assume that $0 < V_A \leq \frac{V_{DD}}{4} \leq V_B \leq \frac{7V_{DD}}{8}$. Find equations and/or inequalities that V_A and V_B should satisfy to avoid signal inversion.





1) If V_{in} is 0V (logic 0), the output of the 1st inverter is V_{DD} (logic 1). The input to the 2nd inverter is $\frac{7V_{DD}}{8}$ in the worst case. Suppose the output of the 2nd inverter is V_2 (which should be logic 0). Then, the input to the 3rd inverter is $V_2 + \frac{V_{DD}}{4}$ in the worst case. If the output of the 3rd inverter is less than V_{DD}, signal inversion will happen in the end.

Thus, $V_2 + \frac{V_{DD}}{4} \leq V_A$.

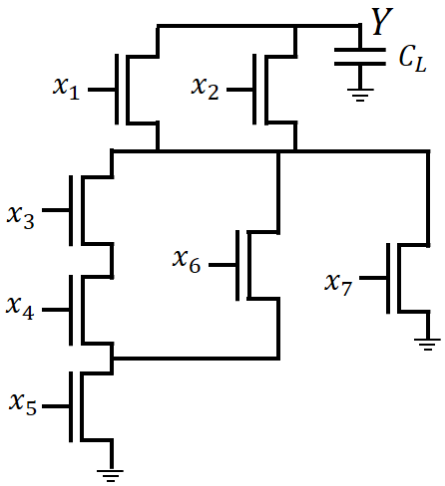
Since $V_B \leq \frac{7V_{DD}}{8}$: $V_2 = 0V$, so $\frac{V_{DD}}{4} \leq V_A$. Since $V_A \leq \frac{V_{DD}}{4}$ in the problem, $V_A = \frac{V_{DD}}{4}$.

2) Similarly, if V_{in} is V_{DD} (logic 1), the output of the 1st inverter is 0 (logic 0). The input to the 2nd inverter is $\frac{V_{DD}}{4}$ in the worst case. Suppose the output of the 2nd inverter is V_3 (which should be logic 1). Then, the input to the 3rd inverter is $V_3 - \frac{V_{DD}}{8}$ in the worst case. If the output of the 3rd inverter is greater than 0V, signal inversion will happen in the end.

Thus, $V_3 - \frac{V_{DD}}{8} \geq V_B$. Since $V_A = \frac{V_{DD}}{4}$, $V_3 = V_{DD}$, so $\frac{7V_{DD}}{8} \geq V_B$.

Problem #4 (Transistor Sizing, 10 points)

Size the transistors in the following NFET network of a static CMOS gate. R_n is the resistance of a 1X NFET. C_L is the load cap. Ignore all the parasitic capacitances. Target timing constraint: $\tau \leq R_n \cdot C_L$. Try to minimize the total area.



Area≤ 24X: 10 points. 24X<Area≤ 26X: 7 points. 26X<Area: 4 points.

x1-x3-x4-x5 is the longest path, so we upsize them to 4X. (total 16X)

x1 and x2 and connected in parallel, so x2 = 4X. (total 20X)

x3-x4 and x6 are connected in parallel, so x6 = 2X. (total 22X)

x1-x7 (or x2-x7): x7 should be 4/3X. (total 23.33X)

x_1: 4X

x_2: 4X

x_3: 4X

x_4: 4X

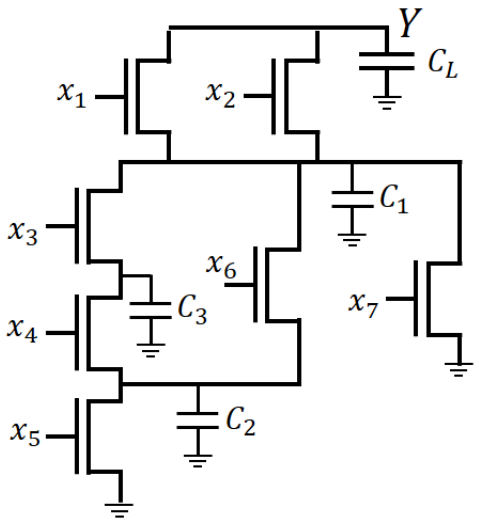
x_5: 4X

x_6: 2X

x_7: $\frac{4}{3}$X

Problem #5 (Switching Characteristics, 15 points)

The following shows the NFET network of a logic gate designed by the static CMOS design methodology. It also shows a load capacitor C_L and three parasitic capacitors C_1, C_2, and C_3. The resistance of transistor x_k is R_k. Assume that all the capacitors are fully charged before we discharge them.



(1) Express the fall delay as a function of R_k and C_m ($k = 1, \ldots, 7$, $m = 1,2,3, L$) for $(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$=(1,0,1,1,1,0,0).

$$\tau = R_5(C_1 + C_2 + C_3 + C_L) + R_4(C_1 + C_3 + C_L) + R_3(C_1 + C_L) + R_1(C_L)$$

(2) Express the fall delay as a function of R_k and C_m ($k = 1, \ldots, 7$, $m = 1,2,3, L$) for $(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$=(1,1,0,0,1,1,0).

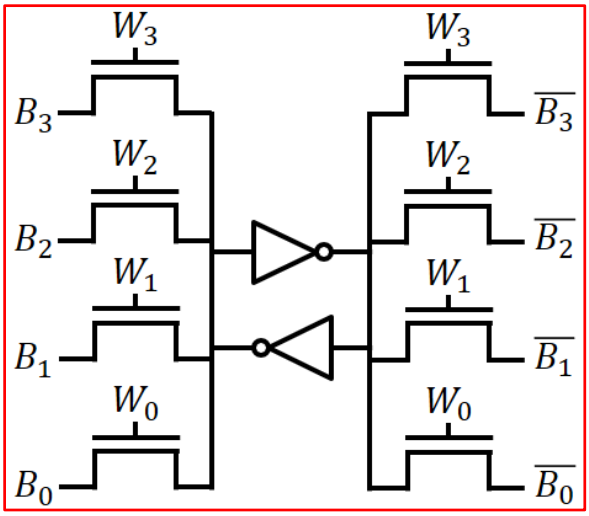
$$\tau = R_5(C_1 + C_2 + C_L) + R_6(C_1 + C_L) + \frac{R_1 R_2}{R_1 + R_2}(C_L)$$

(3) Express the fall delay as a function of R_k and C_m ($k = 1, \ldots, 7$, $m = 1,2,3, L$) for $(x_1, x_2, x_3, x_4, x_5, x_6, x_7)$=(0,1,0,0,0,0,1).

$$\tau = R_7(C_1 + C_L) + R_2 C_L$$

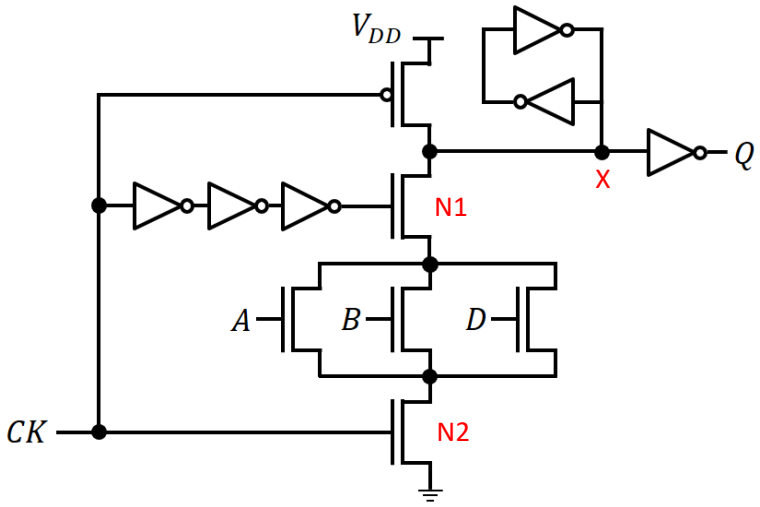
Problem #6 (Memory, 10 points)

We want to design a register file having 16 64-bit registers and supporting four simultaneous accesses (i.e., we can access four different registers at the same time). Draw a 12-transistor SRAM cell supporting the four simultaneous accesses. The Word-line signals are W_0, W_1, W_2, W_3. The four pairs of Bit-line signals are $(B_0, \overline{B_0}), (B_1, \overline{B_1}), (B_2, \overline{B_2}), (B_3, \overline{B_3})$. You should show the Word-line and Bit-line signals too in your figure.



Problem #7 (Flip-Flop, 25 points).

The following schematic shows a positive-edge-triggered D flip-flop. CK is the clock input, Q is the output, and A, B, D are signal inputs. Answer the following questions.



(1) Express the output Q as a function of the input signals A, B, and D.

$Q = A + B + D$ (when CK switches from 0 to 1, the FF captures $A + B + D$).

(2) Explain how you can estimate the setup time of the FF.

(3) Explain how you can estimate the hold time of the FF.

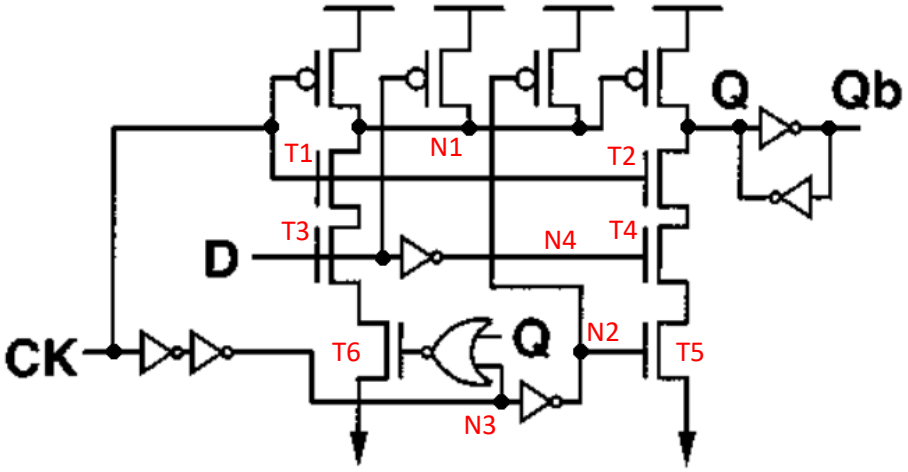
For input A=B=D=0: If CK goes high, N1 will be turned off after the delay of the three inverters. A, B, and D can change after N1 is turned off. Thus, the hold time for this input value combination is the delay of the three inverters.

For input A=1 or B=1 or D=1: If CK goes high, N2 is turned on and node X will be discharged through N1, N2, and the transistors A or B or D. Once we fully discharge node X, A, B, and D can change even if N1 is not turned off. Thus, the hold time for this input value combination is the time to discharge node X. (of course, the delay of the three inverters should be greater than the time to discharge node X.)

For the setup time, A, B, and D can change from 1 to 0 or from 0 to 1 right before a clock rising edge. Thus, the setup time for any input value combination is just some small value.

Problem #8 (Flip-Flop, 25 points).

The following schematic shows a D flip-flop. CK is the clock input, Q is the output, and D is the data input signal. Answer the following questions.



(1) Is it positive-edge-triggered or negative-edge-triggered?

If CK=0, N1 is 1, so Q is isolated and driven by Qb.

For D=0: If CK goes high, T1 and T2 are turned on. T3 is OFF and T4 is ON. N2 was 1 when CK was 1, so Q will be discharged through T2, T4, and T5. N2 will be 0 after some time, so T5 will eventually by turned off.

For D=1: T3 is ON and T4 is OFF. Suppose Q was 0. Then, when CK was 0, T6 was ON. If CK goes high, T1 is turned on, so N1 becomes 0 (discharged through T1, T3, and T6) and Q becomes 1. At the same time, N3 becomes 1, so T6 will eventually be turned off. Suppose Q was 1. Then, T6 was OFF. In this case, even if CK goes high, T6 is still OFF and N1 is 1, but T4 is OFF, so Q will still be 1.

Thus, this is a positive-edge-triggered D-FF.

(2) Explain how you can estimate the setup time of the FF.

(3) Explain how you can estimate the hold time of the FF.

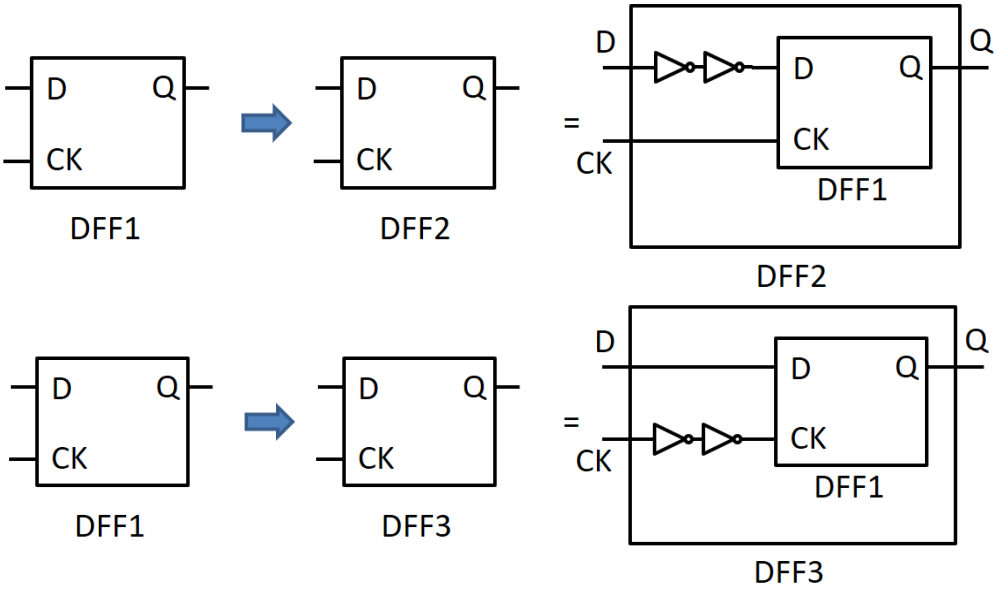
For D=0: D should not change before T5 is turned off. Thus, the hold time for D=0 is the delay of the three inverters. Suppose D is 1, then N4 is 0. If D becomes 0, N4 will become 1 after one inverter delay. Thus, the setup time is the delay of the inverter connected to input D.

For D=1: D can change after N1 is fully discharged. Thus, the hold time for D=1 is the time to discharge node N1 through T1, T3, and T6. Suppose D is 0, then N4 is 1. T4

should be turned off before CK goes high, otherwise Q will be discharged. Turning T4 OFF takes a one-inverter delay. Thus, the setup time is the delay of the inverter connected to input D.

Problem #9 (Flip-Flop, 20 points).

Suppose a D-FF design is given (DFF1) as shown below. Now, we design a new D-FF (DFF2) using a DFF1 as follows. DFF2 has two inverters between the input pin D of DFF2 and the input pin D of DFF1. Similarly, we design a new D-FF (DFF3) using a DFF1 as shown below. Notice that users of DFF2 and DFF3 cannot see the internal designs of DFF2 and DFF3.



- Hold time and setup time of DFF1: h_1 and s_1, respectively
- Hold time and setup time of DFF2: h_2 and s_2, respectively
- Hold time and setup time of DFF3: h_3 and s_3, respectively
- The delay of an inverter: d
- Clock period: T (duty cycle: 50%)

(1) Express h_2 as a function of h_1, s_1, d, T.

$$h_2 = h_1 - 2d$$

(2) Express s_2 as a function of h_1, s_1, d, T.

$$s_2 = s_1 + 2d$$

(3) Express h_3 as a function of h_1, s_1, d, T.

$$h_3 = h_1 + 2d$$

(4) Express s_3 as a function of h_1, s_1, d, T.

$$s_3 = s_1 - 2d$$