

EE466

VLSI System Design

Midterm Exam 2

Nov. 17, 2020. (4:20pm – 5:35pm)

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Name:

WSU ID:

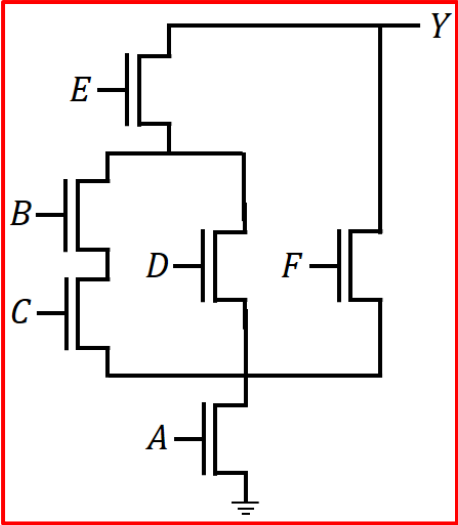
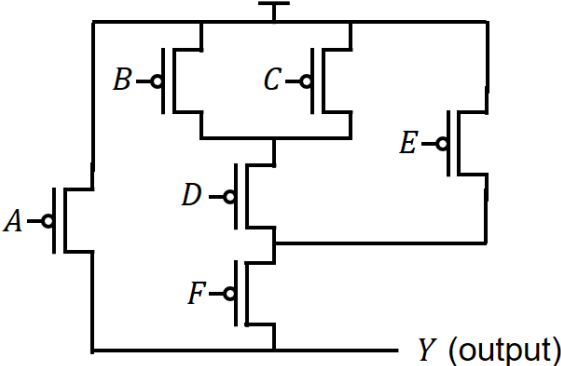
Problem	Points	
1	10	
2	10	
3	10	
4	10	
5	10	
Total	50	

* Allowed: Textbooks, cheat sheets, class notes, notebooks, calculators, watches

* Not allowed: Electronic devices (smart phones, tablet PCs, laptops, etc.) except calculators and watches

Problem #1 (Static CMOS Logic, 10 points).

The following shows the PFET network of a logic gate designed by the static CMOS design methodology. Design the NFET network of the gate (i.e., draw a transistor-level schematic of the NFET network).



Problem #2 (Static CMOS Logic, 10 points).

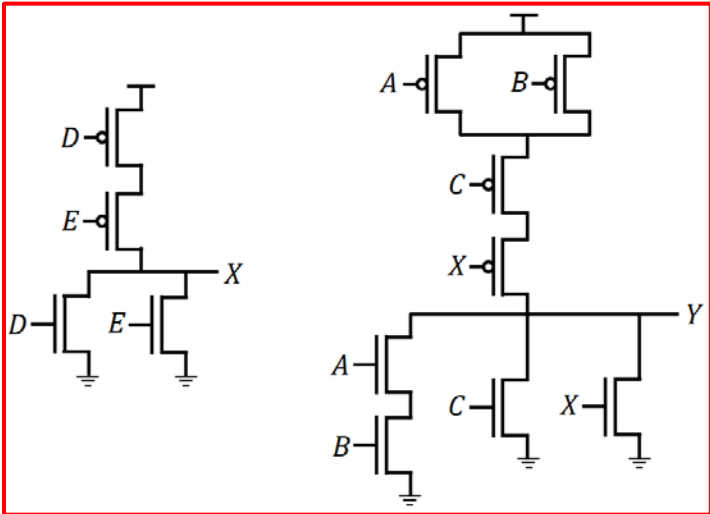
Design the following logic gate using the static CMOS logic design methodology.

$$Y = \overline{(A \cdot B + C)} \cdot (D + E)$$

Available inputs: A, B, C, D, E . Try to minimize # TRs.

If we decompose it into $Y = X \cdot (D + E)$ and $X = \overline{A \cdot B + C}$, we need 6 TRs (for X) + 8 TRs (for Y) = 14 TRs.

We can also design it as follows. $Y = \overline{\overline{(A \cdot B + C)} \cdot (D + E)} = \overline{(A \cdot B + C) + \overline{(D + E)}}$, which requires a two-input NOR gate (4 TRs) and then $\overline{A \cdot B + C + X}$ (8 TRs) = 12 TRs.



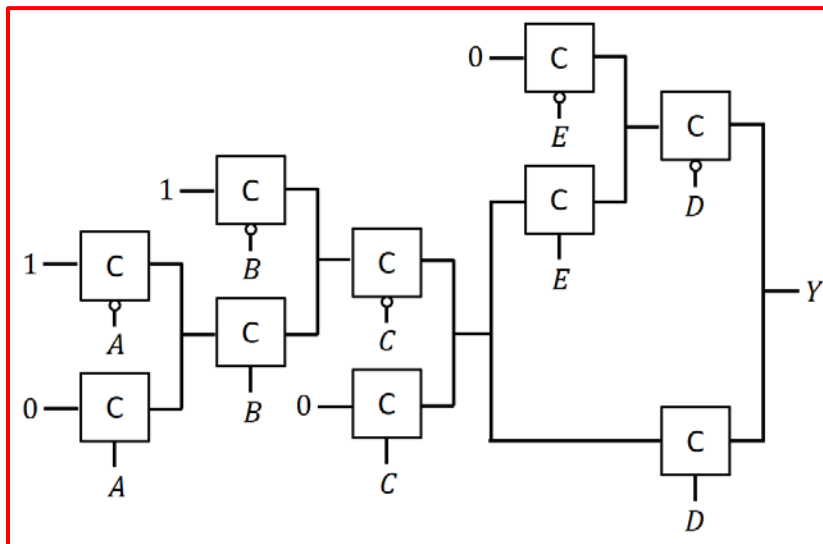
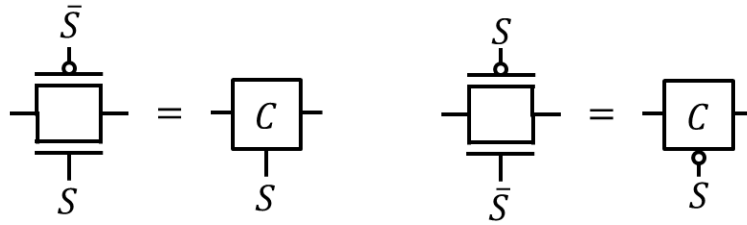
Problem #3 (Transmission Gates, 10 points).

Design the following logic gate using transmission gates (TGs).

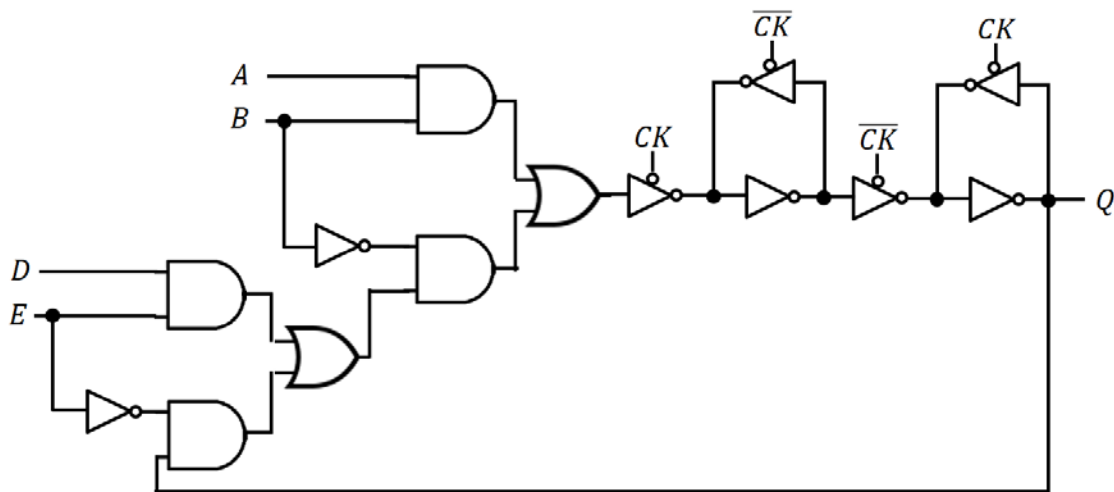
$$Y = \overline{(A \cdot B + C)} \cdot (D + E)$$

Available inputs: A, B, C, D, E (and VDD and GND). Use the following symbols for the TGs.

≤12 TGs: 10 points. ≤14 TGs: 7 points. ≤16 TGs: 5 points. Otherwise: 3 points.



Problem #4 (Logic Analysis, 10 points).



This logic gate is a flip-flop (D is the a input, CK is a clock input, and A, B, E are some additional inputs.) Describe the functionality of the flip-flop in as much detail as possible (e.g., whether it is positive-edge-triggered, negative-edge-triggered, or dual-edge, and what A does, etc.).

If E is 0, D is suppressed. On the other hand, if E is 1, the Q signal fed back to the input is suppressed.

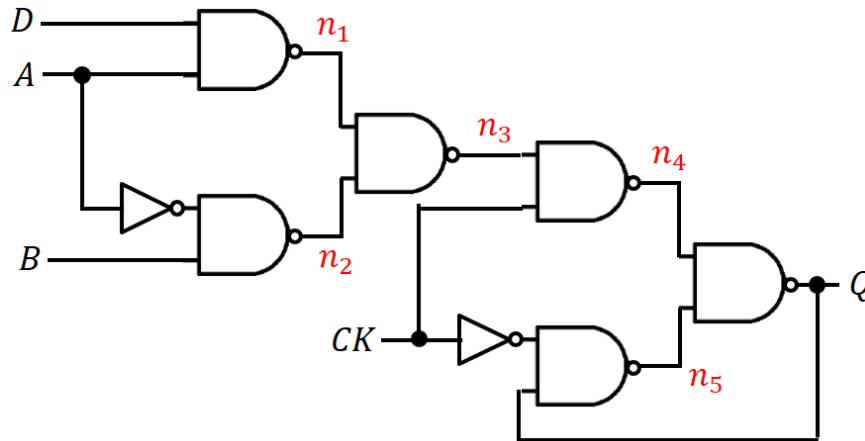
If B is 1, A goes into the body of the FF. If B is 0, then either D or Q (depending on E) goes into the body of the FF.

If CK is 0, Q holds the current value. When CK switches from 0 to 1, the FF captures the input.

=> Thus, this is a positive-edge-triggered D-F/F. If B is 1, A is captured. If B is 0 and E is 1, D is captured. If B is 0 and E is 0, it doesn't capture any input signal (so Q just holds the current value.)

Problem #5 (Static CMOS Logic, 10 points).

This logic gate is a sequential logic (D is a data input, CK is a clock input, and A, B are some additional inputs.) Describe the functionality of the gate in as much detail as possible.



If A is 0, B is fed into the body. If A is 1, D is fed into the body. Thus, A is like an input signal selector.

Suppose A is 1. Then, n_2 is 1 and n_1 is \bar{D} , so n_3 is D . Similarly, if A is 0, n_3 will be B .

If CK is 0, n_4 is 1 and n_5 is \bar{Q} , so $Q=Q$, i.e., Q holds the current value. If CK is 1, n_4 is $\bar{n_3}$ and n_5 is 1, so $Q=\bar{n_4} = n_3$, which is either B or D depending on A .

Thus, this is a positive latch (i.e., positive level-sensitive latch) with a signal selector A . If A is 0, $Q=B$ when $CK=high$. If A is 1, $Q=D$ when $CK=high$. If $CK=low$, Q holds the current value.