EE466

VLSI System Design

Final Exam

Dec. 13, 2021. (7:30pm – 9:30pm)

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Name:

WSU ID:

Problem	Points	
1	30	
2	20	
3	80	
4	20	
5	20	
6	30	
Total	200	

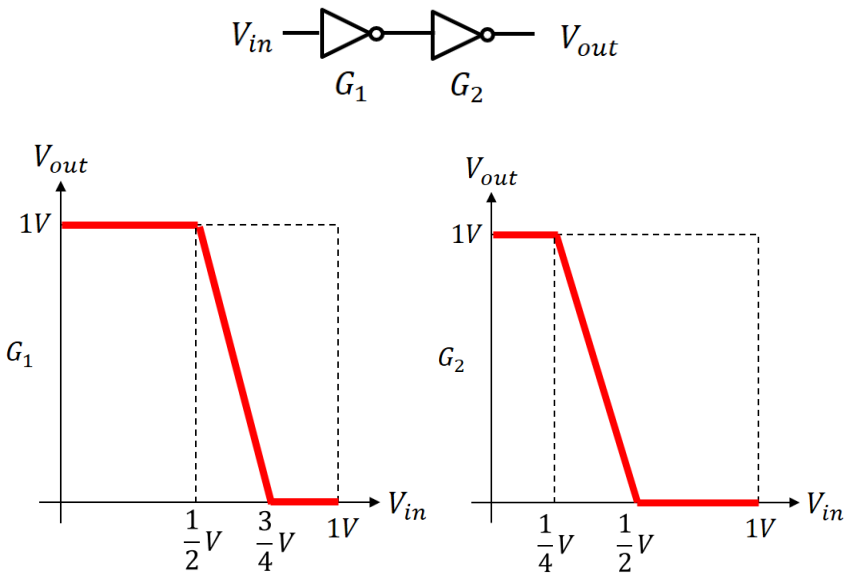
* Allowed: Textbooks, cheat sheets, class notes, notebooks, calculators, watches

* Not allowed: Electronic devices (smart phones, tablet PCs, laptops, etc.) except calculators and watches

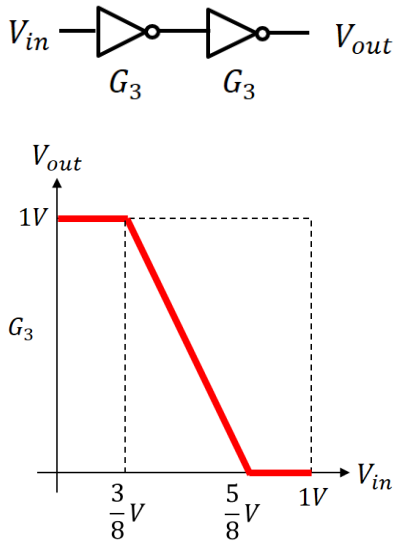
Problem #1 (DC Analysis, 30 points)

We will compare the following two buffers, BUF1 and BUF2.

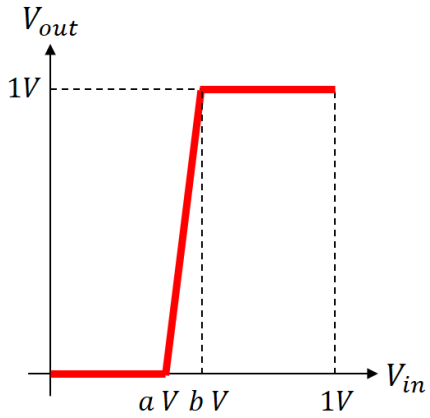
BUF1: (composed of two inverters, G1 and G2. Their DC curves are shown below.)



BUF2: (composed of two identical inverters, G3. Its DC curve is shown below.)



Notice that the DC curves of the buffers will look like this:

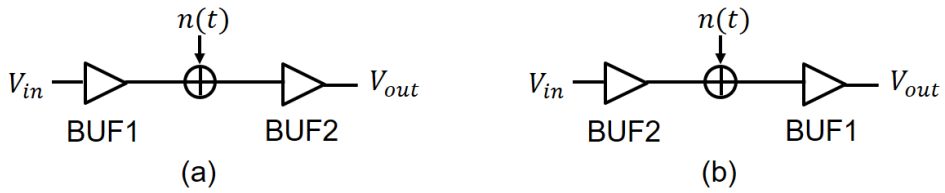


Answer the following questions.

(1) Find $a\ (V)$ and $b\ (V)$ for BUF1. (10 points)

(2) Find $a\ (V)$ and $b\ (V)$ for BUF2. (10 points)

(3) The following figure shows two configurations of two cascaded buffers. $n(t)$ is a noise source. Answer the following questions (Correct: +2 points, Wrong: -2 points, no answer: 0 points, minimum: 0 points, maximum: 10 points).



(3-a) If $n(t)$ is +0.4V, configuration (a) has a signal inversion problem for $V_{in} = 0V$. (True / False)

(3-b) If $n(t)$ is +0.4V, configuration (b) has a signal inversion problem for $V_{in} = 0V$. (True / False)

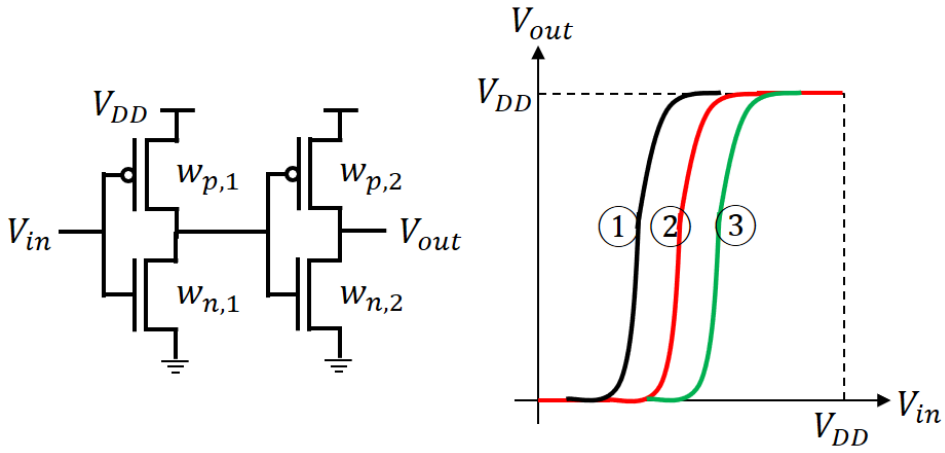
(3-c) If $n(t)$ is +0.6V, configuration (a) has a signal inversion problem for $V_{in} = 0V$. (True / False)

(3-d) If $n(t)$ is +0.6V, configuration (b) has a signal inversion problem for $V_{in} = 0V$. (True / False)

(3-e) If $n(t)$ is -0.4V, configuration (b) has a signal inversion problem for $V_{in} = 1V$. (True / False)

Problem #2 (DC Analysis, 20 points)

The following figure shows a buffer composed of two inverters (left) and its DC characteristic curve (② in the right figure) for $w_{n,1} = w_{n,2} = w_1$ and $w_{p,1} = w_{p,2} = w_2$.



Answer the following questions (Correct: +5 points, Wrong: -2 points, no answer: 0 points, minimum: 0 points, maximum: 20 points).

(1) If we increase $w_{n,1}$, the DC curve is shifted from ② to ①. (True / False)

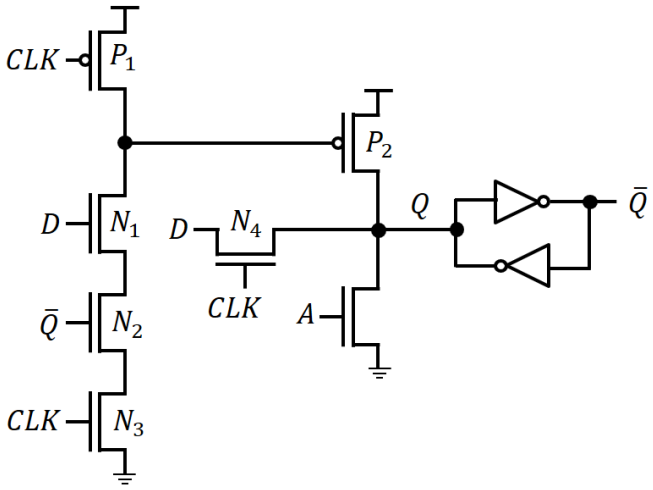
(2) If we increase $w_{n,2}$, the DC curve is shifted from ② to ①. (True / False)

(3) If we increase $w_{p,1}$, the DC curve is shifted from ② to ①. (True / False)

(4) If we increase $w_{p,2}$, the DC curve is shifted from ② to ①. (True / False)

Problem #3 (D Flip Flop, 80 points)

The following schematic implements a D FF. Answer the following questions. Assume that all the setup and hold times are positive (≥0). You can also assume that T_{CLK} is the clock period and the duty cycle is 50% (i.e., the clock is high for $\frac{T_{CLK}}{2}$ and low for $\frac{T_{CLK}}{2}$.)



(1) Is it positive-edge-triggered or negative-edge-triggered or dual-edge-triggered or positive-level-sensitive or negative-level-sensitive? (5 points)

(2) What does signal A do? Describe its function in detail. (5 points)

(3) Estimate the setup time of the FF for $D = 0$. (10 points)

(4) Estimate the setup time of the FF for $D = 1$. (10 points)

(5) Estimate the hold time of the FF for $D = 0$. (10 points)

(6) Estimate the hold time of the FF for $D = 1$. (10 points)

(7) True/False questions. Correct: +5 points, Wrong: -5 points, no answer: 0 points, minimum: 0 points.

(a) If the width of N_1 goes up, the fall delay of the FF goes down. (True / False)

(b) If the width of N_2 goes up, the fall delay of the FF goes down. (True / False)

(c) If the width of N_3 goes up, the fall delay of the FF goes down. (True / False)

(d) If the width of N_4 goes up, the fall delay of the FF goes down. (True / False)

(e) If the width of P_1 goes up, the rise delay of the FF goes down. (True / False)

(f) If the width of P_2 goes up, the rise delay of the FF goes down. (True / False)

Problem #4 (Logic Design, 20 points)

Design the following logic gate using NFETs and PFETs. Try to minimize the # TRs.
Available input signals: A, B, C

$$Y = A \cdot B + (A \oplus C)$$

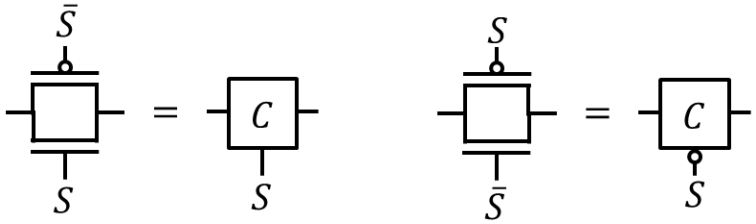
≤18 TRs: 20 points. ≤20 TRs: 16 points. ≤22 TRs: 12 points. Otherwise: 10 points.

Problem #5 (Transmission Gates, 20 points).

Design the following logic gate using transmission gates (TGs).

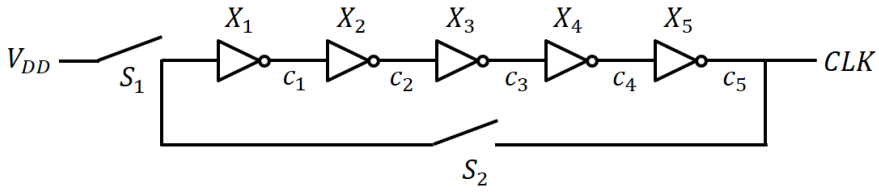
$$Y = A \cdot B + D \cdot (E \oplus F)$$

Available inputs: A, B, D, E, F (and 0 and 1). Use the following symbols for the TGs.



≤10 TGs: 20 points. ≤12 TGs: 17 points. ≤14 TGs: 15 points. Otherwise: 12 points.

Problem #6 (Ring Oscillator, 30 points)



The figure shown above implements a ring oscillator. It consists of five inverters and two ideal switches. First, S1 is closed and S2 is open so that $c_1 = 0, c_2 = 1, c_3 = 0, c_4 = 1,$ and $c_5 = 0$. Then, we open S1 and close S2 so that we can initiate the oscillation. In this case, $c_5 = 0$ is fed into X_1, so c_1 becomes 1, $c_2 = 0$, ..., $c_5 = 1$. This can be used for a clock source as shown above.

Parameters/Constants:

- p_k: The delay of the PFET of Inverter X_k. For example, p_2 is the delay of the PFET of X_2, which is actually the time spent to charge node c_2 to V_{DD}.
- n_k: The delay of the NFET of Inverter X_k. For example, n_4 is the delay of the NFET of X_4, which is actually the time spent to discharge node c_4 to 0.
- Ignore all the parasitic RC.

Answer the following questions.

(1) Express the period (T_{CLK}) of the CLK signal as a function of $p_1, p_2, \dots, p_5, n_1, \dots, n_5$. (10 points)

(2) The duty cycle of a clock signal is defined as the time it is high (logical value 1) divided by its period. For example, if a clock signal is high for 0.25ns and low for 0.75ns, the duty cycle is 0.25ns / (0.25ns + 0.75ns) = 0.25 (or 25%).

Find the duty cycle of the clock signal generated by the ring oscillator (Express the duty cycle using the constants). (10 points)

(3) If net c_4 (instead of net c_5) is used for the clock source, what is the duty cycle of the new clock signal? Express it as a function of the given constants. (10 points)