

EE466

VLSI System Design

Midterm Exam

Oct. 7, 2020. (4:20pm – 5:35pm)

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Name:

WSU ID:

Problem	Points	
1	10	
2	10	
3	10	
4	10	
5	20	
6	10	
7	10	
Total	80	

* Allowed: Textbooks, cheat sheets, class notes, notebooks, calculators, watches

* Not allowed: Electronic devices (smart phones, tablet PCs, laptops, etc.) except calculators and watches

Problem #1 (Kogge-Stone Adder, 10 points).

For the 1024-bit Kogge-Stone adder, show one of the critical paths to calculate S_{139} . What is the delay of the critical path? Use the following delay values for logic gates.

- 2-, 3-, 4-input AND, OR: d
- XOR: $3d$

Problem #2 (Carry-Lookahead Adder, 10 points).

For the 1024-bit Carry-lookahead adder, show one of the critical paths to calculate S_{139} . What is the delay of the critical path? Use the following delay values for logic gates.

- 2-, 3-, 4-input AND, OR: d
- XOR: $3d$

Problem #3 (Conditional Sum Adder, 10 points)

Complete the following table.

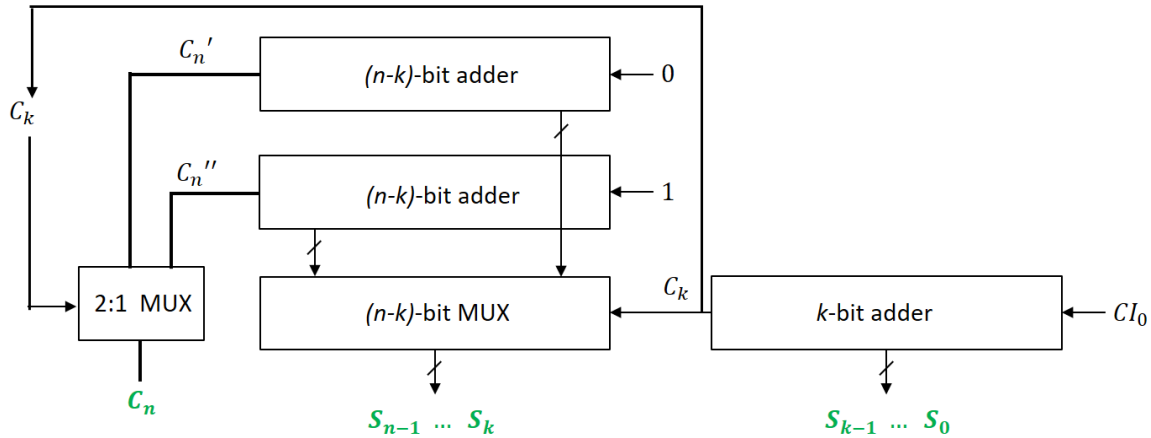
	$i:$	7	6	5	4	3	2	1	0
	$A_i:$	1	1	1	1	0	1	0	0
	$B_i:$	1	0	1	1	1	1	0	1
Step 1	$S_i^0:$								
	$CO_i^0:$								
Step 1	$S_i^1:$								
	$CO_i^1:$								
Step 2	$S_i^0:$								
	$CO_i^0:$								
Step 2	$S_i^1:$								
	$CO_i^1:$								
Step 3	$S_i^0:$								
	$CO_i^0:$								
Step 3	$S_i^1:$								
	$CO_i^1:$								
Step 4	$S_i^0:$								
	$CO_i^0:$								
Step 4	$S_i^1:$								
	$CO_i^1:$								

Problem #4 (Carry-Lookahead Adder, 10 points)

For the 256-bit carry-lookahead adder, the input is $A_{255:0}$ and $B_{255:0}$ and the output is $S_{255:0}$ and C_{256} . We can calculate the delay of each sum bit S_k using the techniques we studied. How many among the 256 sum bits have the longest delay? You can estimate the number (i.e., the number doesn't need to be very accurate. Just a good estimation will be enough to get 10 points). Use the following assumptions for the delay calculation.

- 2-, 3-, 4-input AND, OR: d
- XOR: $2d$

Problem #5 (Hybrid Adder, 20 points)



The figure above shows an n -bit carry-select adder. We split it into two groups, the first $(n - k)$ bits and the second k bits as shown. The k -bit adder is a ripple-carry adder and the two $(n - k)$ -bit adders are carry-lookahead adders. We want to find the optimal value of k to minimize the total delay. Answer the following questions using the following assumptions.

- Delay of a 2-, 3-, and 4-input AND (or OR) gate: d
- Delay of a full adder (FA): $2d$
- Delay of an XOR gate: $2d$
- Delay of a 1-bit MUX: $2d$

- (1) Since the delay of an FA is $2d$, the delay of the carry-out signal C_k is _____.
- (2) The delay of a g_i signal is _____.
- (3) The delay of a p_i signal is _____.
- (4) The delay of a $g_{i:i-3}$ signal is _____.
- (5) The delay of a $g_{i:i-15}$ signal is _____.
- (6) The delay of a $g_{i:i-(4^m-1)}$ signal is _____.
- (7) The delay of a C_{4^m-1} (or $C_{2 \cdot 4^m-1}$ or $C_{3 \cdot 4^m-1}$) signal is _____.
- (8) The delay of a C_{4^m-2} (or $C_{2 \cdot 4^m-2}$ or $C_{3 \cdot 4^m-2}$) signal is _____.
- (9) The delay of a C_{4t} (t is a generally large integer) signal is _____.
- (10) The delay of a C_{4t+1} (or C_{4t+2} or C_{4t+3}) signal is _____.

(11) The delay of a S_{4t+1} (or S_{4t+2} or S_{4t+3}) signal is _____.

(12) If $(n - k)$ can be represented approximately by 4^m , m is _____ (represent it using n and k).

(13) Thus, the delay of an $(n - k)$ -bit CLA is approximately _____.

Hint, note: The longest delay of the whole carry-select adder is minimized when the longest delay of the $(n - k)$ -bit adder is equal to the delay of C_k . This requires solving the following equation (expressing k with respect to n).

$$2 \log_4(n - k) = k - 1$$

We can't solve it analytically, but we can numerically.

For $n = 64$, optimal k is approximately 6.

For $n = 256$, optimal k is approximately 8.

For $n = 1,024$, optimal k is approximately 10.

Problem #6 (Wallace Tree, 10 points)

(1) If you multiply two 3-bit unsigned binary numbers, how many carry-save-adder stages do you need to reduce the number of partial product rows down to two?

(2) Repeat it for two 4-bit unsigned binary numbers.

(3) Repeat it for two 5-bit unsigned binary numbers.

Problem #7 (Modified Booth Encoding, 10 points)

Use the modified Booth encoding technique to calculate the following multiplication (see page 9 in the multiplier lecture notes). Assume that all the numbers are unsigned.

$$\begin{array}{r} A \quad \quad 01101101 \\ * X \quad \quad 00111001 \\ \hline \end{array}$$