EE466

VLSI System Design

Final Exam

Dec. 14, 2022. (7:30pm – 9:30pm)

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Name:

WSU ID:

Problem	Points	
1	80	
2	20	
3	70	
4	40	
5	20	
Total	230	

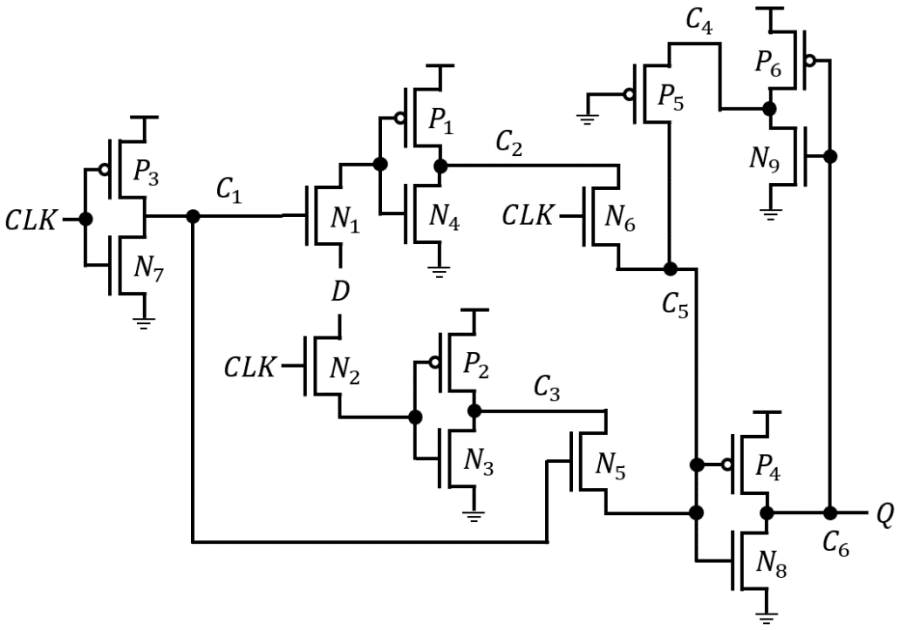
* Allowed: Textbooks, cheat sheets, class notes, notebooks, calculators, watches

* Not allowed: Electronic devices (smart phones, tablet PCs, laptops, etc.) except calculators and watches

Problem #1 (DFF, 80 points)

The following schematic implements a D FF. Answer the following questions. Assume that all the setup and hold times are positive (≥0). You can also assume that T_{CLK} is the clock period and the duty cycle is 50% (i.e., the clock is high for $\frac{T_{CLK}}{2}$ and low for $\frac{T_{CLK}}{2}$.)

Use C_1 to C_6 for the capacitances of the nets shown in the figure. If a net does not have $C_{\#}$, then you can ignore the capacitance of the net. Use $R_{N\#}$ (or $R_{P\#}$) for the resistance the NFET N# (or PFET P#).



For D=0, Q=1, CLK goes high: $C_1 = 0$. N_1 is OFF. C_2 was 1, so C_5 becomes 1 (VDD-Vtn). $C_3 = 1$. N_8 is ON, so $C_6 = 0$, so Q=0. $C_4 = 1$, which pulls up C_5 to VDD.

For D=1, Q=0, CLK goes high: $C_1 = 0$. N_1 is OFF. C_2 was 0, so C_5 becomes 0. $C_3 = 0$. P_4 is ON, so $C_6 = 1$, so Q=1. $C_4 = 0$.

For D=0, Q=1, CLK goes low: $C_3 = 1$. N_5 is ON. C_5 becomes 1 (VDD-Vtn), so C_6 becomes 0, so Q=0. $C_4 = 1$, which pulls up C_5 to VDD.

For D=1, Q=0, CLK goes low: $C_3 = 0$. N_5 is ON. C_5 becomes 0, so C_6 becomes 1, so Q=1. $C_4 = 0$.

(1) Is it (positive-edge-triggered) or (negative-edge-triggered) or (dual-edge-triggered) or (positive-level-sensitive) or (negative-level-sensitive)? (10 points)

Dual-edge-triggered

(2) Estimate the setup time of the FF for $D = 0$ and $CLK = \nearrow$. (10 points)

Suppose D=1 when CLK=0. Then, N_4 is ON, so $C_2 = 0$. Now, if D becomes 0, P_1 should be turned on so that C_2 becomes 1. Thus, D becomes 0 → Turn on P_1 (delay = $R_{N1} \cdot C_{in}$) → Charge C_2 (delay = $R_{P1} \cdot C_2$). Then, it is safe for CLK to go high.

Thus, the setup time is $\boldsymbol{R_{N1} \cdot C_{in} + R_{P1} \cdot C_2}$ where C_{in} is the input capacitance of the inverter composed of P_1 and N_4.

(3) Estimate the setup time of the FF for $D = 1$ and $CLK = \nearrow$. (10 points)

Suppose D=0 when CLK=0. Then, P_1 is ON, so $C_2 = 1$. Now, if D becomes 1, N_4 should be turned on so that C_2 becomes 0. Thus, D becomes 1 → Turn on N_4 (delay = $R_{N1} \cdot C_{in}$) → Discharge C_2 (delay = $R_{N4} \cdot C_2$). Then, it is safe for CLK to go high.

Thus, the setup time is $\boldsymbol{R_{N1} \cdot C_{in} + R_{N4} \cdot C_2}$ where C_{in} is the input capacitance of the inverter composed of P_1 and N_4.

(4) Estimate the hold time of the FF for $D = 0$ and $CLK = \nearrow$. (10 points)

CLK goes high → C_1 goes low, then the change of D does not go through P_1 or N_4 or N_5. Thus, the hold time is $\boldsymbol{R_{N7} \cdot C_1}$.

(5) Estimate the hold time of the FF for $D = 1$ and $CLK = \nearrow$. (10 points)

This is the same as (4). $\boldsymbol{R_{N7} \cdot C_1}$.

(6) Estimate the rise delay of the FF for $CLK = \nearrow$. (10 points)

For D=1 and Q=0, $C_2 = 0$ and $C_5 = 1$. If CLK goes high, then C_5 is discharged through N_6 and N_4. Then, P_4 is turned on and C_6 is charged by P_4. Thus, the rise delay is approximately $\boldsymbol{(R_{N4} + R_{N6}) \cdot C_5 + R_{P4} \cdot C_6}$.

(7) Estimate the fall delay of the FF for $CLK = \nearrow$. (10 points)

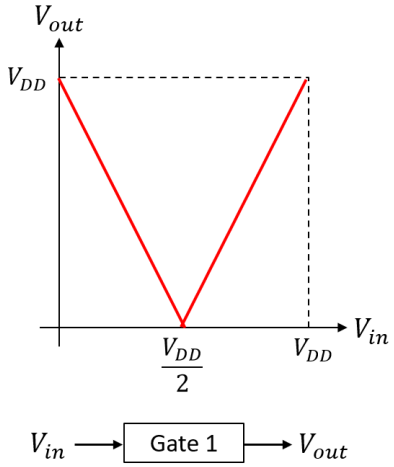
For D=0 and Q=1, $C_2 = 1$ and $C_5 = 0$. If CLK goes high, then C_5 is charged through N_6 and P_1. Then, N_8 is turned on and C_6 is discharged by N_8. Thus, the fall delay is approximately $\boldsymbol{(R_{P1} + R_{N6}) \cdot C_5 + R_{N8} \cdot C_6}$.

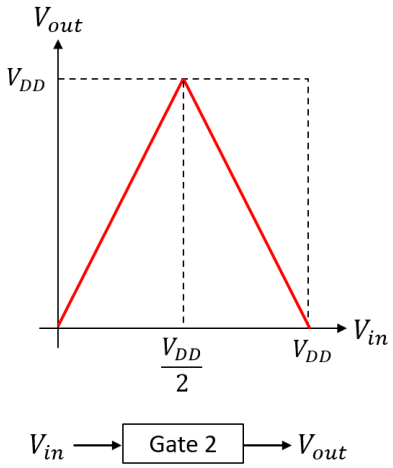
(8) Estimate the power consumption of the FF for $D = 0$ and $CLK = \nearrow$. (10 points)

If CLK goes high, C_1 is discharged. Power = $0.5C_1{V_{DD}}^2$. $C_2 = 1$, so $0.5C_2{V_{DD}}^2$. $C_5 = 1$, so $0.5C_5{V_{DD}}^2$. For the output, $0.5C_6{V_{DD}}^2$. C_4 is charged too, so $0.5C_4{V_{DD}}^2$. Thus, the power is $0.5(C_1 + C_2 + C_4 + C_5 + C_6){V_{DD}}^2$.

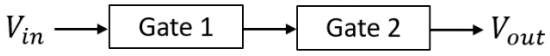
Problem #2 (DC Analysis, 20 points)

The following shows two gates (Gate 1 and Gate 2) and their DC characteristics.

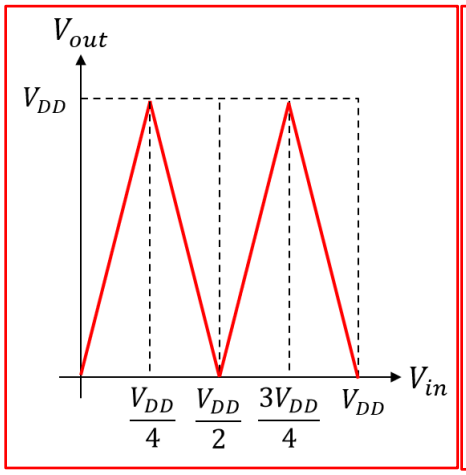


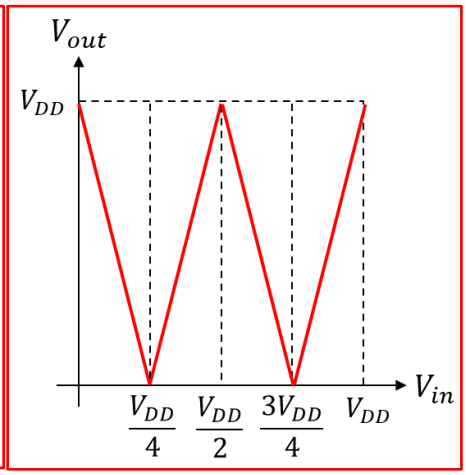


Draw a DC characteristic curve for the following gate. (10 points)

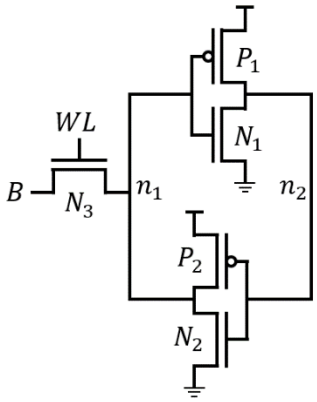


Also, draw a DC characteristic curve for the following gate. (10 points)





Problem #3 (Memory, 70 points)



The figure above shows a 5T SRAM cell. When we write a logic value 1 to the cell, we set B to V_{DD} and $\bar{B}$ to 0V. Similarly, when we write a logic value 0 to the cell, we set B and $\bar{B}$ to 0V and V_{DD}, respectively.

- Threshold voltage of an NFET (or PFET): V_{tn} (or V_{tp}).
- ON resistance of NFET $N_{\#}$ (or PFET $P_{\#}$): $R_{n\#}$ (or $R_{p\#}$).
- Capacitance of node $n_{\#}$: $C_{\#}$.

(1) Show an inequality to be able to write a logical value 1 to the cell. (10 points)

$n_1 = 0$ and $n_2 = 1$. When, $B = 1$, N_3 and N_2 form a resistive network between V_{DD} and GND. If n_1 can be charged to V_{tn}, then N_1 will be turned on, so n_2 decreases from V_{DD} to $V_{DD} - \delta$, which will start turning off N_2. Thus, $V_{DD} \cdot \frac{R_{n2}}{R_{n2}+R_{n3}} \geq V_{tn}$.

(2) Show an inequality to be able to write a logical value 0 to the cell. (10 points)

$n_1 = 1$ and $n_2 = 0$. When, $B = 0$, N_3 and P_2 form a resistive network between V_{DD} and GND. If n_1 can be discharged to $V_{DD} - |V_{tp}|$, then P_1 will be turned on, so n_2 increases from 0 to δ, which will start turning off P_2. Thus, $V_{DD} \cdot \frac{R_{n3}}{R_{n3}+R_{p2}} \leq V_{DD} - |V_{tp}|$.

(3) Suppose the cell has a logical value 0. We write a logical value 1 to the cell and then write a logical value 0 to the cell. Estimate the total energy consumption (use C_1 and C_2). (10 points)

$$(C_1 + C_2){V_{DD}}^2$$

Answer the following questions. Correct: +4 points, Wrong: -4 points, No answer: 0 points, Min: 0 points. You can ignore the parasitic capacitances of the transistors.

(4) If we increase the width of P_1, the delay for writing 1 to the cell goes down. (Yes / No)

(5) If we increase the width of N_1, the delay for writing 1 to the cell goes down. (Yes / No)

(6) If we increase the width of P_2, the delay for writing 1 to the cell goes down. (Yes / No)

(7) If we increase the width of N_2, the delay for writing 1 to the cell goes down. (Yes / No)

(8) If we increase the width of N_3, the delay for writing 1 to the cell goes down. (Yes / No)

(9) If we increase the width of P_1, the delay for writing 0 to the cell goes down. (Yes / No)

(10) If we increase the width of N_1, the delay for writing 0 to the cell goes down. (Yes / No)

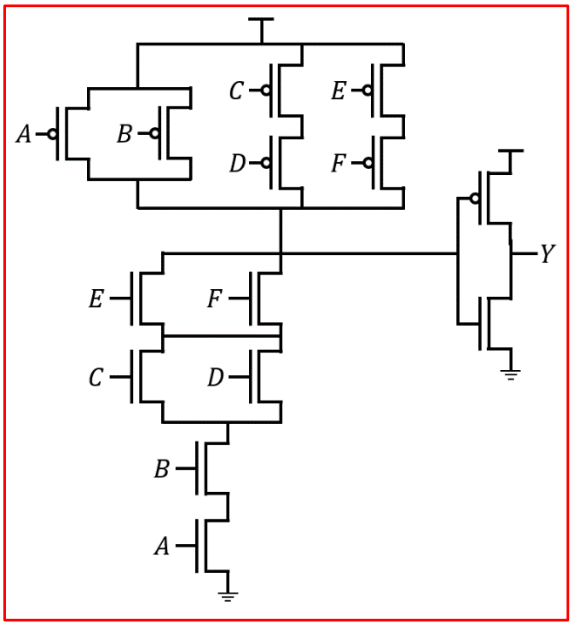
(11) If we increase the width of P_2, the delay for writing 0 to the cell goes down. (Yes / No)

(12) If we increase the width of N_2, the delay for writing 0 to the cell goes down. (Yes / No)

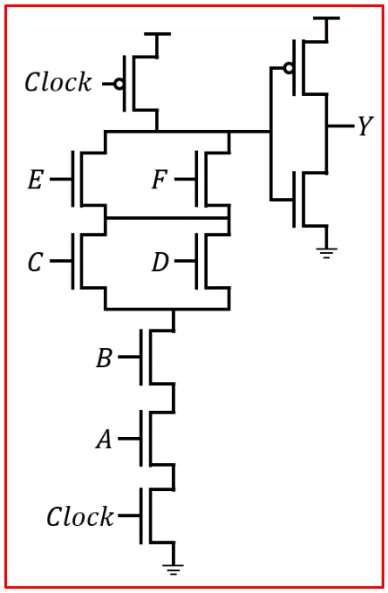
(13) If we increase the width of N_3, the delay for writing 0 to the cell goes down. (Yes / No)

Problem #4 (Logic Design, 40 points)

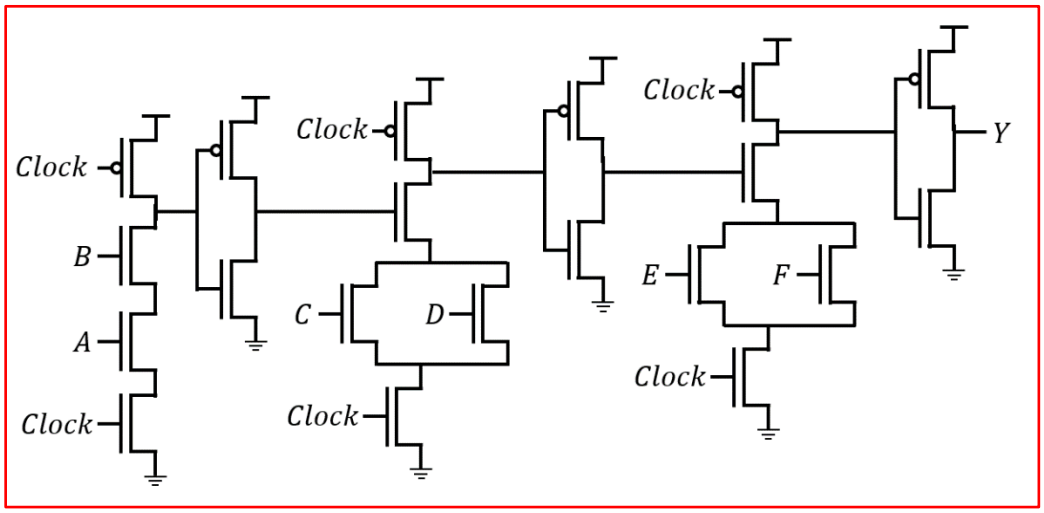
(1) Design $Y = \{A \cdot B \cdot (C + D)\} \cdot (E + F)$. Available input: A, B, C, D, E, F. Use the static CMOS design methodology (draw a schematic). (10 points)



(2) Design Y using the dynamic CMOS design methodology (draw a schematic). Available input: $A, B, C, D, E, F, clock, \overline{clock}$. You can ignore charge sharing. (10 points)

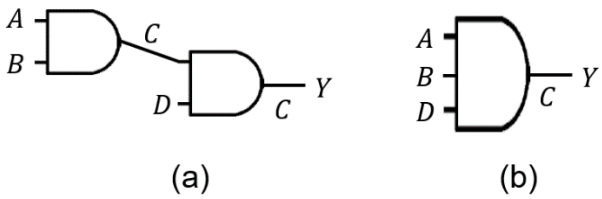


(3) Now, you have a design constraint, “the number of NFETs connected in series in any discharging path from any (internal) output to the ground should be less than or equal to three.” Design Y using the domino logic technique (draw a schematic). Available input: $A, B, C, D, E, F, clock, \overline{clock}$. Ignore charge sharing. Try to minimize # TRs in your design. (20 points)



Problem #5 (Energy, 20 points)

The following shows two different designs for $Y = A \cdot B \cdot D$.



(a) (b)

C is the capacitance of each net. You can ignore parasitic capacitances inside the gates.

A, B, and D switch from 0 to 1 or from 1 to 0, or just stay at 0 or 1. The probabilities of 0→0 (staying at 0), 0→1, 1→0, and 1→1 (staying at 1) are all equal (25%). Compare the energy consumption of (a) and (b).

For (a)

n stays at 0: (A,B)=(0,0)→(0,0), (0,1), (1,0). (0,1)→(0,0), (0,1), (1,0). (1,0)→(0,0), (0,1), (1,0). = 9/16

n stays at 1: (A,B)=(1,1)→(1,1). = 1/16

n switches from 0 to 1: (A,B) switches from (0,0), (0,1), (1,0) to (1,1). = 3/16

n switches from 1 to 0: (A,B) switches from (1,1) to (0,0), (0,1), (1,0). = 3/16.

Y switches from 0 to 1: (n,D) switches from (0,0), (0,1), (1,0) to (1,1).

Y switches from 1 to 0: (n,D) switches from (1,1) to (0,0), (0,1), (1,0).

(n,D): (0,0)→(1,1): 3/16 * 1/4 = 3/64

(n,D): (0,1)→(1,1): 3/16 * 1/4 = 3/64

(n,D): (1,0)→(1,1): 1/16 * 1/4 = 1/64

Thus, Y switches from 0 to 1 with the probability of 7/64. Similarly, Y switches from 1 to 0 with the probability of 7/64. Y's switching probability: 14/64.

n's switching probability: 6/16.

Thus, the energy consumption is $\left(\frac{14}{64}+\frac{6}{16}\right) \cdot C \cdot {V_{DD}}^2 = \frac{38}{64} C {V_{DD}}^2$

For (b)

Y switches from 0 to 1: (A,B,D): (0,0,0), (0,0,1), (0,1,0), (0,1,1), (1,0,0), (1,0,1), (1,1,0)→(1,1,1). = 7/64

Similarly, Y switches from 1 to 0: = 7/64.

Thus, the energy consumption is $\left(\frac{7}{64}+\frac{7}{64}\right)\cdot C\cdot {V_{DD}}^2=\frac{14}{64}C{V_{DD}}^2$