EE466

VLSI System Design

Final Exam

Dec. 14, 2022. (7:30pm – 9:30pm)

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Name:

WSU ID:

Problem	Points	
1	80	
2	20	
3	70	
4	40	
5	20	
Total	230	

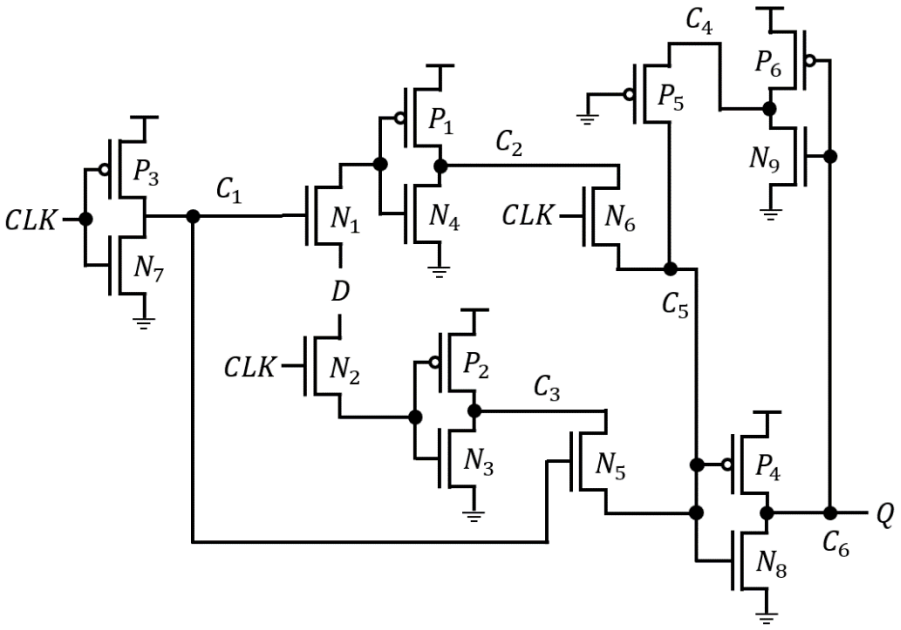
* Allowed: Textbooks, cheat sheets, class notes, notebooks, calculators, watches

* Not allowed: Electronic devices (smart phones, tablet PCs, laptops, etc.) except calculators and watches

Problem #1 (DFF, 80 points)

The following schematic implements a D FF. Answer the following questions. Assume that all the setup and hold times are positive (≥0). You can also assume that T_{CLK} is the clock period and the duty cycle is 50% (i.e., the clock is high for $\frac{T_{CLK}}{2}$ and low for $\frac{T_{CLK}}{2}$.)

Use C_1 to C_6 for the capacitances of the nets shown in the figure. If a net does not have $C_{\#}$, then you can ignore the capacitance of the net. Use $R_{N\#}$ (or $R_{P\#}$) for the resistance the NFET N# (or PFET P#).



(1) Is it (positive-edge-triggered) or (negative-edge-triggered) or (dual-edge-triggered) or (positive-level-sensitive) or (negative-level-sensitive)? (10 points)

(2) Estimate the setup time of the FF for $D = 0$ and $CLK = \nearrow$. (10 points)

(3) Estimate the setup time of the FF for $D = 1$ and $CLK = \nearrow$. (10 points)

(4) Estimate the hold time of the FF for $D = 0$ and $CLK = \nearrow$. (10 points)

(5) Estimate the hold time of the FF for $D = 1$ and $CLK = \nearrow$. (10 points)

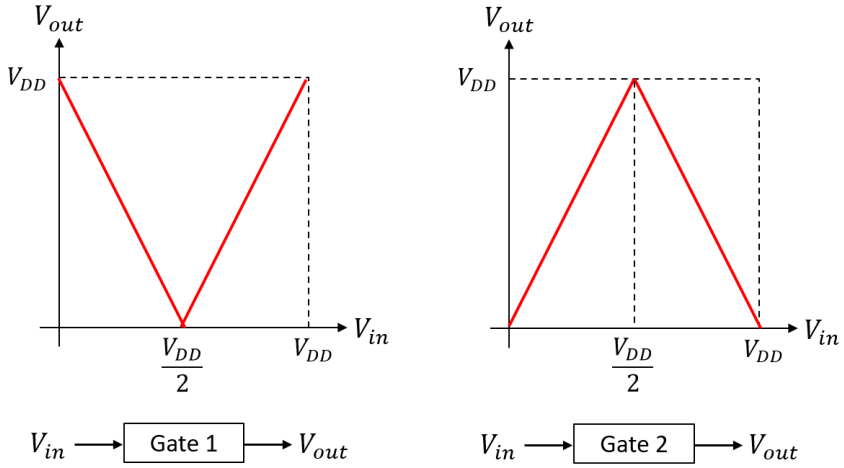
(6) Estimate the rise delay of the FF for $CLK = \nearrow$. (10 points)

(7) Estimate the fall delay of the FF for $CLK = \nearrow$. (10 points)

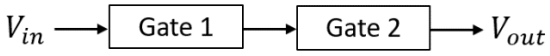
(8) Estimate the power consumption of the FF for $D = 0$ and $CLK = \nearrow$. (10 points)

Problem #2 (DC Analysis, 20 points)

The following shows two gates (Gate 1 and Gate 2) and their DC characteristics.

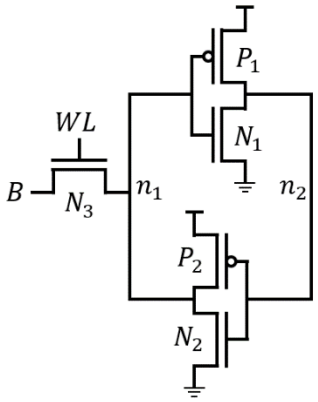


Draw a DC characteristic curve for the following gate. (10 points)



Also, draw a DC characteristic curve for the following gate. (10 points)

Problem #3 (Memory, 70 points)



The figure above shows a 5T SRAM cell. When we write a logic value 1 to the cell, we set B to V_{DD} and $\bar{B}$ to 0V. Similarly, when we write a logic value 0 to the cell, we set B and $\bar{B}$ to 0V and V_{DD}, respectively.

- Threshold voltage of an NFET (or PFET): V_{tn} (or V_{tp}).
- ON resistance of NFET $N_{\#}$ (or PFET $P_{\#}$): $R_{n\#}$ (or $R_{p\#}$).
- Capacitance of node $n_{\#}$: $C_{\#}$.

(1) Show an inequality to be able to write a logical value 1 to the cell. (10 points)

(2) Show an inequality to be able to write a logical value 0 to the cell. (10 points)

(3) Suppose the cell has a logical value 0. We write a logical value 1 to the cell and then write a logical value 0 to the cell. Estimate the total energy consumption (use C_1 and C_2). (10 points)

Answer the following questions. Correct: +4 points, Wrong: -4 points, No answer: 0 points, Min: 0 points. You can ignore the parasitic capacitances of the transistors.

(4) If we increase the width of P_1, the delay for writing 1 to the cell goes down. (Yes / No)

(5) If we increase the width of N_1, the delay for writing 1 to the cell goes down. (Yes / No)

(6) If we increase the width of P_2, the delay for writing 1 to the cell goes down. (Yes / No)

(7) If we increase the width of N_2, the delay for writing 1 to the cell goes down. (Yes / No)

(8) If we increase the width of N_3, the delay for writing 1 to the cell goes down. (Yes / No)

(9) If we increase the width of P_1, the delay for writing 0 to the cell goes down. (Yes / No)

(10) If we increase the width of N_1, the delay for writing 0 to the cell goes down. (Yes / No)

(11) If we increase the width of P_2, the delay for writing 0 to the cell goes down. (Yes / No)

(12) If we increase the width of N_2, the delay for writing 0 to the cell goes down. (Yes / No)

(13) If we increase the width of N_3, the delay for writing 0 to the cell goes down. (Yes / No)

Problem #4 (Logic Design, 40 points)

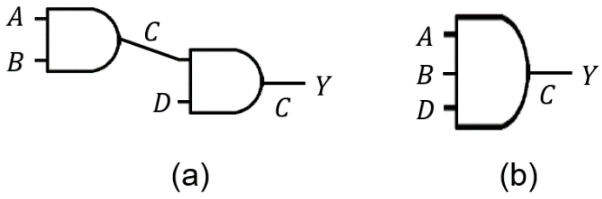
(1) Design $Y = \{A \cdot B \cdot (C + D)\} \cdot (E + F)$. Available input: A, B, C, D, E, F. Use the static CMOS design methodology (draw a schematic). (10 points)

(2) Design Y using the dynamic CMOS design methodology (draw a schematic). Available input: $A, B, C, D, E, F, clock, \overline{clock}$. You can ignore charge sharing. (10 points)

(3) Now, you have a design constraint, "the number of NFETs connected in series in any discharging path from any (internal) output to the ground should be less than or equal to three." Design Y using the domino logic technique (draw a schematic). Available input: $A, B, C, D, E, F, clock, \overline{clock}$. Try to minimize # TRs in your design. (20 points)

Problem #5 (Energy, 20 points)

The following shows two different designs for $Y = A \cdot B \cdot D$.



(a) (b)

C is the capacitance of each net. You can ignore parasitic capacitances inside the gates.

A, B, and D switch from 0 to 1 or from 1 to 0, or just stay at 0 or 1. The probabilities of 0→0 (staying at 0), 0→1, 1→0, and 1→1 (staying at 1) are all equal (25%). Compare the energy consumption of (a) and (b).