EE466

VLSI System Design

Midterm Exam

Nov. 11, 2022. (4:20pm – 5:35pm)

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Name:

WSU ID:

Problem	Points	
1	10	
2	10	
3	10	
4	10	
5	20	
6	10	
7	10	
Total	80	

* Allowed: Textbooks, cheat sheets, class notes, notebooks, calculators, watches

* Not allowed: Electronic devices (smart phones, tablet PCs, laptops, etc.) except calculators and watches

Problem #1 (Kogge-Stone Adder, 10 points)

For the 128-bit Kogge-Stone adder, show one of the critical paths to calculate S_{77}. What is the delay of the critical path? Use the following delay values for logic gates.

- 2-input AND, OR: d
- XOR: 2d

Problem #2 (Kogge-Stone Adder, 20 points)

Count the # following gates required to implement the 16-bit Kogge-Stone adder (including the generation of C_{16}).

- 2-input AND gates:
- 2-input OR gates:
- 2-input XOR gates:

Problem #3 (Carry-Lookahead Adder, 10 points)

For the 128-bit Carry-lookahead adder, show one of the critical paths to calculate S_{77}. What is the delay of the critical path? Use the following delay values for logic gates.

- 2-, 3-, 4-input AND, OR: d
- XOR: 2d

Problem #4 (Carry-Lookahead Adder, 20 points)

Count the # following gates required to implement the 16-bit Carry-Lookahead adder (including the generation of C_{16}).

- 2,3,4-input AND gates (i.e., # 2-input ANDs + # 3-input ANDs + # 4-input ANDs):
- 2,3,4-input OR gates:
- 2-input XOR gates:

Problem #5 (Ripple-Carry Adder, 10 points)

For the 128-bit ripple-carry adder, estimate the delay of the critical path to compute S_{127}. Use the following delay values for logic gates.

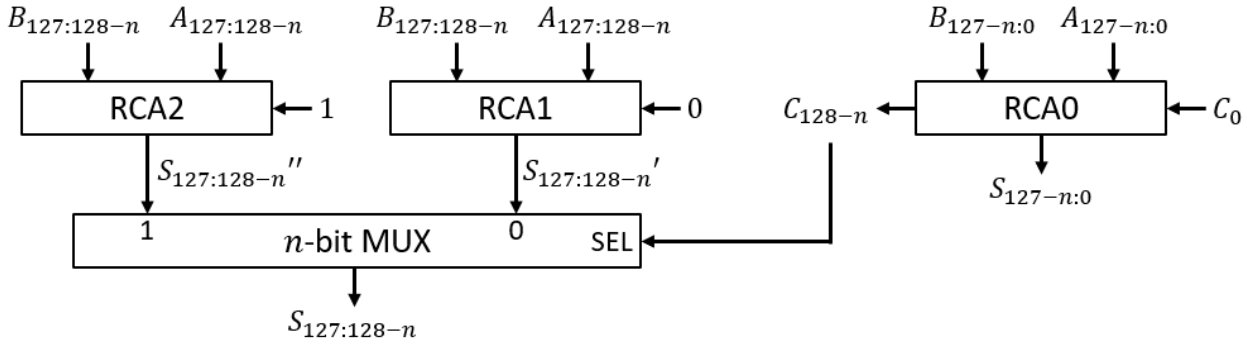
- 2-input AND, OR: d
- XOR: 2d

Use the following expressions for the computation of each carry signal.

- $g_i = A_i \cdot B_i$
- $p_i = A_i \oplus B_i$
- $C_{i+1} = g_i + p_i \cdot C_i$
- $S_i = p_i \oplus C_i$

Problem #6 (Ripple-Carry Adder, 20 points)

We want to design a 128-bit adder as follows. First, we split it into n bits (MSBs) and $128 - n$ bits (LSBs). Then, we add $A_{127-n:0}$, $B_{127-n:0}$, and C_0 using a $(128 - n)$-bit ripple-carry adder (RCA0). At the same time, we add $A_{127:128-n}$, $B_{127:128-n}$, 0 in an n-bit RCA (RCA1), and also add $A_{127:128-n}$, $B_{127:128-n}$, 1 in another n-bit RCA (RCA2). The following shows a schematic of this adder.



Use the following delay values for logic gates.

- 2-input AND, OR: d
- XOR: 2d
- MUX: 3d

Use the following expressions for the computation of each carry signal.

- $g_i = A_i \cdot B_i$
- $p_i = A_i \oplus B_i$
- $C_{i+1} = g_i + p_i \cdot C_i$
- $S_i = p_i \oplus C_i$

(1) Calculate the delay of C_{128-n}. (Note: It should include n.)

(2) Calculate the delay of ${S_{127}}'$. (Note: It should include n.)

(3) Calculate the delay of S_{127} for $n = 64$. (Note: the delay of ${S_{127}}''$ is equal to that of ${S_{127}}'$.)

(4) Calculate the delay of S_{127} for $n > 64$. (Note: It should include n.)

Problem #7 (Prefix Adder, 10 points)

Count the # following gates required to implement the 16-bit Brent-Kung adder shown below (including the generation of C_{16}).

- 2-input AND gates:
- 2-input OR gates:
- 2-input XOR gates: