EE466

VLSI System Design

Final Exam

Dec. 11, 2023. (4:30pm – 6:30pm)

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Name:

WSU ID:

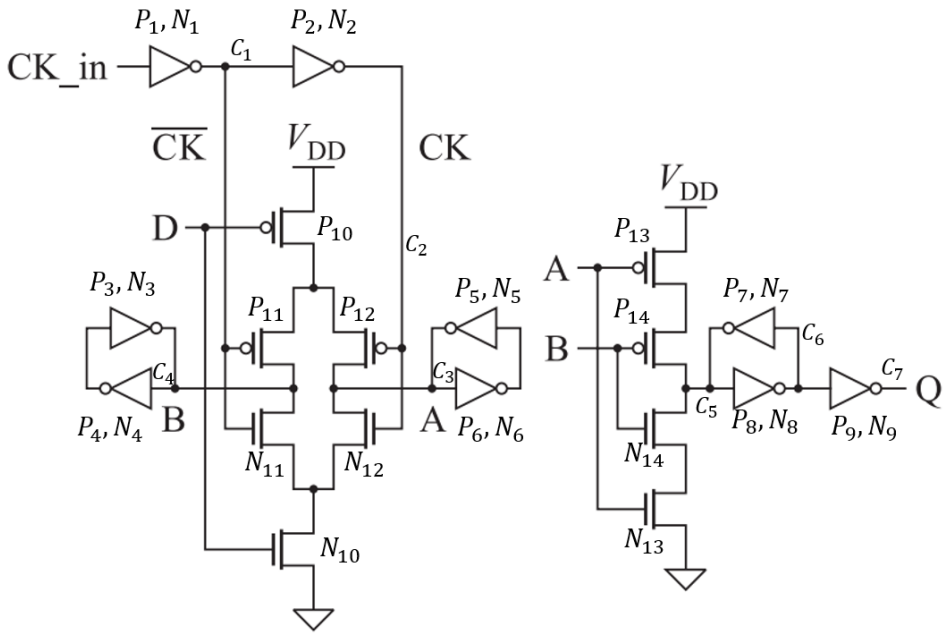
Problem	Points	
1	80	
2	20	
3	50	
4	20	
5	30	
Total	200	

* Allowed: Textbooks, cheat sheets, class notes, notebooks, calculators, watches

* Not allowed: Electronic devices (smart phones, tablet PCs, laptops, etc.) except calculators and watches

Problem #1 (DFF, 80 points)

The following schematic shows a dual-edge D flip flop. Answer the following questions. Assume that all the setup and hold times are positive (≥0). You can also assume that T_{CLK} is the clock period and the duty cycle is 50% (i.e., the clock is high for $\frac{T_{CLK}}{2}$ and low for $\frac{T_{CLK}}{2}$.) Use C_1 to C_7 for the capacitances of the nets shown in the figure. If a net does not have $C_{\#}$, then you can ignore the capacitance of the net. Use $R_{N\#}$ (or $R_{P\#}$) for the resistance of the NFET N# (or PFET P#). For example, R_{N1} is the resistance of N_1.



Fall: CLK=0 and D=0. Then, $A = 1$. If CLK goes high, P_{11} is ON, so $B = 1$ (A holds the previous value, 1). Now, A and B are 1, so C_5 becomes 0, C_6 becomes 1, and Q becomes 0.

Rise: CLK=0 and D=1. Then, $B = 0$. If CLK goes high, N_{12} is ON, so $A = 0$ (B holds the previous value, 0). Now, A and B are 0, so C_5 becomes 1, C_6 becomes 0, and Q becomes 1.

(1) Estimate the fall delay of the FF for $CLK = \nearrow$. (10 points)

- The first inverter discharges C_1: $R_{N1} \cdot C_1$
- P_{11} is turned ON and C_4 (B) is charged: $(R_{P10} + R_{P11}) \cdot C_4$
- C_5 is discharged (notice that when CK=0, A=1, so N_{13} was ON): $(R_{N13} + R_{N14}) \cdot C_5$
- C_6 is charged: $R_{P8} \cdot C_6$
- C_7 is discharged: $R_{N9} \cdot C_7$

Delay = $R_{N1} \cdot C_1 + (R_{P10} + R_{P11}) \cdot C_4 + (R_{N13} + R_{N14}) \cdot C_5 + R_{P8} \cdot C_6 + R_{N9} \cdot C_7$

(2) Estimate the rise delay of the FF for $CLK = \nearrow$. (10 points)

- The first inverter discharges C_1: $R_{N1} \cdot C_1$
- The second inverter charges C_2: $R_{P2} \cdot C_2$
- N_{12} is turned ON and C_3 (A) is discharged: $(R_{N10} + R_{N12}) \cdot C_3$
- C_5 is charged (notice that when CK=0, A=0, so P_{13} was ON): $(R_{P13} + R_{P14}) \cdot C_5$
- C_6 is discharged: $R_{N8} \cdot C_6$
- C_7 is charged: $R_{P9} \cdot C_7$

Delay = $R_{N1} \cdot C_1 + R_{P2} \cdot C_2 + (R_{N10} + R_{N12}) \cdot C_3 + (R_{P13} + R_{P14}) \cdot C_5 + R_{N8} \cdot C_6 + R_{P9} \cdot C_7$

(3) Estimate the setup time of the FF for $D = 0$ and $CLK = \nearrow$. (10 points)

Suppose D=1 when CLK=0. Then, B=0. (A holds its previous value.) Now, if D becomes 0, then A is charged to 1. If CLK goes high, then B also becomes 1, which discharges C_5. Thus, A must be fully charged to 1 before C_2 goes high. The time to charge C_3 is $(R_{P10} + R_{P12}) \cdot C_3$. Thus, the setup time is

If $R_{N1} \cdot C_1 + R_{P2} \cdot C_2 - (R_{P10} + R_{P12}) \cdot C_3 > 0$, then 0.

If $R_{N1} \cdot C_1 + R_{P2} \cdot C_2 - (R_{P10} + R_{P12}) \cdot C_3 < 0$, then $(R_{P10} + R_{P12}) \cdot C_3 - R_{N1} \cdot C_1 - R_{P2} \cdot C_2$.

Setup time = MAX(0, $(R_{P10} + R_{P12}) \cdot C_3 - R_{N1} \cdot C_1 - R_{P2} \cdot C_2$).

(4) Estimate the setup time of the FF for $D = 1$ and $CLK = \nearrow$. (10 points)

Suppose D=0 when CLK=0. Then, A=1. (B holds its previous value.) Now, if D becomes 1, then B is discharged to 0. If CLK goes high, then A also becomes 0, which charges C_5. Thus, B must be fully discharged to 0 before C_1 goes low. The time to discharge C_4 is $(R_{N10} + R_{N11}) \cdot C_4$. Thus, the setup time is

If $R_{N1} \cdot C_1 - (R_{N10} + R_{N11}) \cdot C_4 > 0$, then 0.

If $R_{N1} \cdot C_1 - (R_{N10} + R_{N11}) \cdot C_4 < 0$, then $(R_{N10} + R_{N11}) \cdot C_4 - R_{N1} \cdot C_1$.

Setup time = MAX(0, $(R_{N10} + R_{N11}) \cdot C_4 - R_{N1} \cdot C_1$).

(5) Estimate the hold time of the FF for $D = 0$ and $CLK = \nearrow$. (10 points)

CLK=0 and D=0 (so A=1). CLK goes high $\rightarrow$ C_1 goes low, then P_{11} is turned on and B=1. At the same time, C_2 goes high and N_{12} is turned on. Now, B=1 discharges C_5. If D switches from 0 to 1, then N_{10} is turned ON, so A is discharged to 0 and C_5 will be driven by the cross-coupled inverters. Thus, D can change after C_5 is discharged.

Hold time = $R_{N1} \cdot C_1 + (R_{P10} + R_{P11}) \cdot C_4 + (R_{N13} + R_{N14}) \cdot C_5$

(6) Estimate the hold time of the FF for $D = 1$ and $CLK = \nearrow$. (10 points)

CLK=0 and D=1 (so B=0). CLK goes high $\rightarrow C_2$ goes high, then N_{12} is turned on and A=0, which charges C_5. If D switches from 1 to 0, then P_{10} is turned ON, so B is charged to 1 and C_5 will be driven by the cross-coupled inverters. Thus, D can change after C_5 is charged.

Hold time = $R_{N1} \cdot C_1 + R_{P2} \cdot C_2 + (R_{N10} + R_{N12}) \cdot C_3 + (R_{P13} + R_{P14}) \cdot C_5$

(7) Estimate the energy consumption of the FF for $D = 0$ and $CLK = \nearrow$. (10 points)

From the fall delay calculation, we discharge C_1, charge C_2, charge C_4, discharge C_5, charge C_6, and discharge C_7, so the total energy consumption is

$$0.5(C_1 + C_2 + C_4 + C_5 + C_6 + C_7){V_{DD}}^2$$

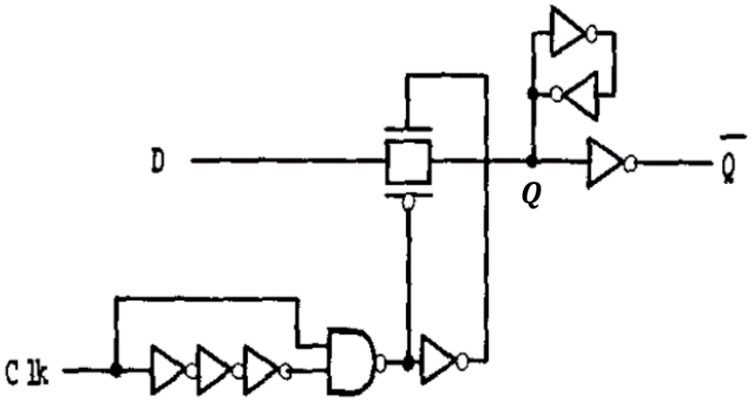
(8) Estimate the energy consumption of the FF for $D = 1$ and $CLK = \nearrow$. (10 points)

From the rise delay calculation, we discharge C_1,charge C_2, discharge C_3, charge C_5, discharge C_6, and charge C_7, so the total energy consumption is

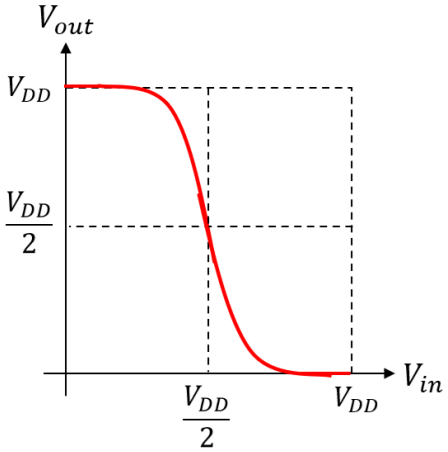
$$0.5(C_1 + C_2 + C_3 + C_5 + C_6 + C_7){V_{DD}}^2$$

Problem #2 (DC Analysis, 20 points)

The following shows an explicitly-pulsed hybrid static flip-flop (ep-SFF) design.

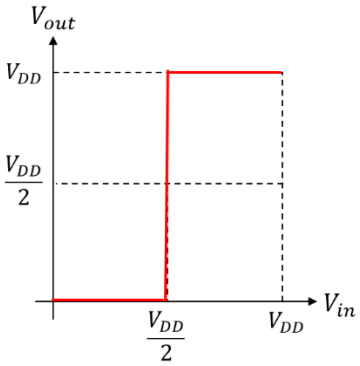


The following shows the DC characteristics of all the inverters in the figure.

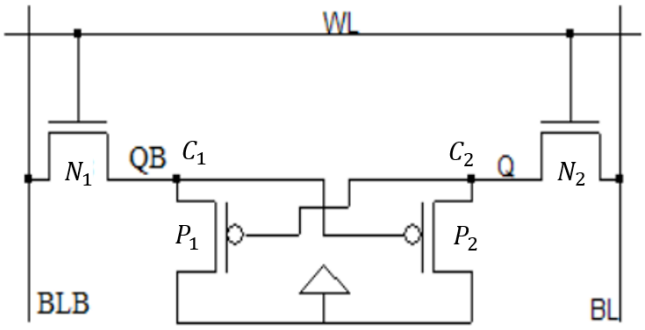


Draw a DC characteristic curve (Q vs. D) for the above DFF.

When CLK goes high, D is transmitted to Q. When the transmission gate is disabled, the cross-coupled inverters will set Q to 0 or VDD.



Problem #3 (Memory, 50 points)



The figure above shows a 4T SRAM cell (WL: Word line, BL: Bit line, BLB: Inverted bit line). When we write a logic value 1 to the cell, we set BL to V_{DD} and $\overline{BL}$ to 0V. Similarly, when we write a logic value 0 to the cell, we set BL and $\overline{BL}$ to 0V and V_{DD}, respectively. (The triangle denotes VDD).

- Threshold voltage of an NFET (or PFET): V_{tn} (or V_{tp}).
- ON resistance of NFET $N_{\#}$ (or PFET $P_{\#}$): $R_{n\#}$ (or $R_{p\#}$).
- Capacitance of a net: $C_{\#}$ (shown above).
- Assume $V_{tn} > |V_{tp}|$

(1) Show an inequality to be able to write a logical value 1 to the cell. (10 points)

Suppose QB=1 and Q=0 (so previously it stored 0). Now, set BL=1 and BL'=0, and turn on WL. When N1 and N2 are turned on, Q=1 (VDD-Vtn,2) and QB=0, so P2 is ON and P1 is OFF, so Q is charged to VDD through P2. This is how it works.

Now, if N1 is turned on, QB is discharged through N1, so P1 and N1 forms a voltage divider. If QB is not low enough, we can't turn on P2. This condition is

$$V_{DD} - V_{DD} \cdot \frac{R_{N1}}{R_{P1} + R_{N1}} > |V_{tp}|$$

or, you can turn off P1. This condition is

$$V_{DD} - V_Q < |V_{tp}|$$

, but the max. of V_Q is $V_{DD} - V_{tn}$, so the above condition is $V_{tn} < |V_{tp}|$, but this is false by the given assumption. Thus, the first condition is the only condition.

(2) Show an inequality to be able to write a logical value 0 to the cell. (10 points)

$$V_{DD} - V_{DD} \cdot \frac{R_{N2}}{R_{P2} + R_{N2}} > |V_{tp}|$$

(3) Suppose the cell has a logical value 0. We write a logical value 1 to the cell and then write a logical value 0 to the cell. Estimate the total energy consumption (use C_1 and C_2). (10 points)

$$(C_1 + C_2){V_{DD}}^2$$

Answer the following questions. Correct: +5 points, Wrong: -5 points, No answer: 0 points, Min: 0 points. You can ignore the parasitic capacitances of the transistors.

(4) If we increase the width of P_1, the delay for writing 1 to the cell goes down. (True / **False**)

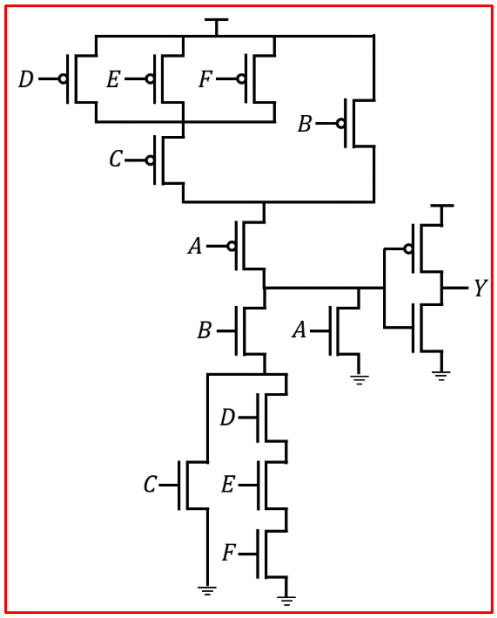
(5) If we increase the width of N_1, the delay for writing 1 to the cell goes down. (**True** / False)

(6) If we increase the width of P_2, the delay for writing 1 to the cell goes down. (**True** / False)

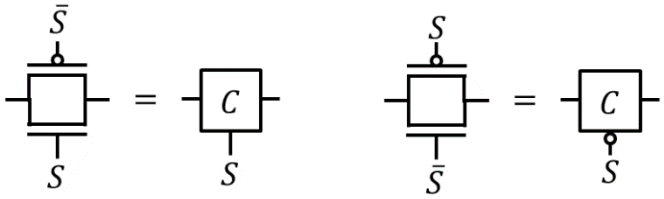
(7) If we increase the width of N_2, the delay for writing 1 to the cell goes down. (**True** / False)

Problem #4 (Logic Design, 20 points)

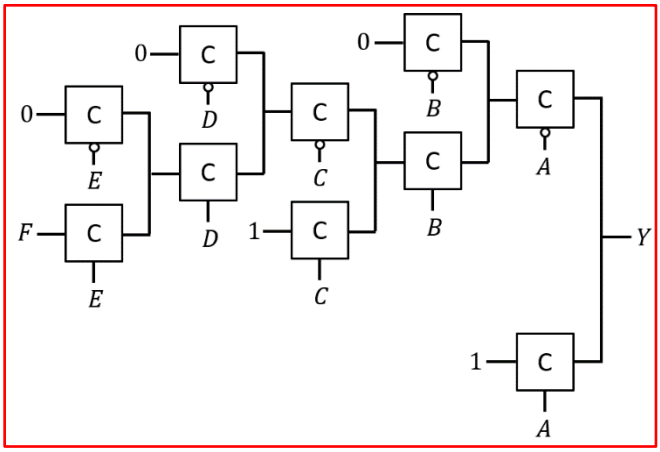
(1) Design $Y = A + B \cdot (C + D \cdot E \cdot F)$. Available input: A, B, C, D, E, F. Use the static CMOS design methodology (draw a schematic). (10 points)



(2) Design Y using transmission gates. Available inputs: A, B, C, D, E, F (and 0 and 1). Use the following symbols for the transmission gates. (10 points)

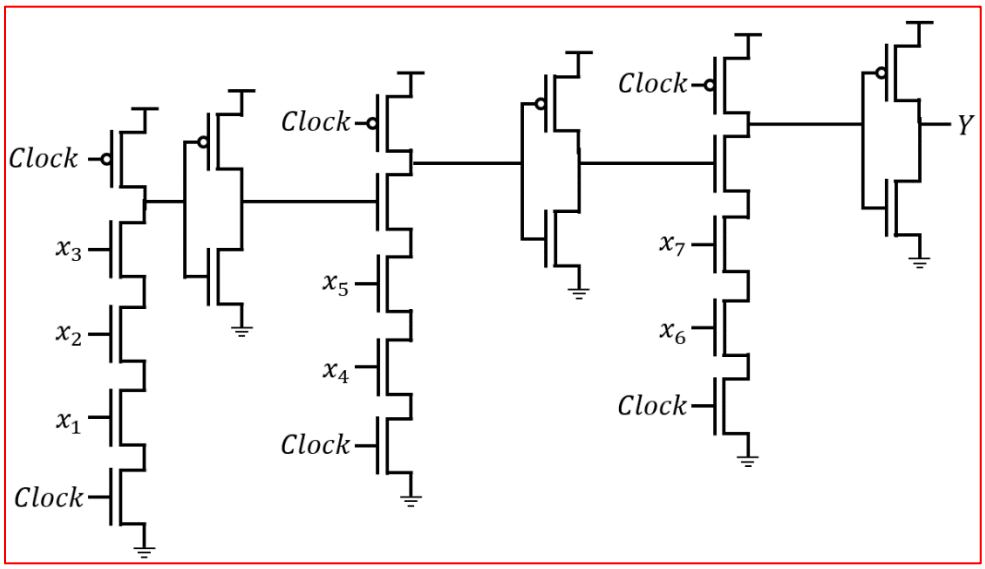


≤10 TGs: 10 points. ≤12 TGs: 8 points. ≤14 TGs: 6 points. Otherwise: 5 points.



Problem #5 (Domino Logic, 30 points)

(1) Design a domino-logic-based 7-input AND gate, $Y = x_1 \cdot x_2 \cdot \ldots \cdot x_7$ (draw a schematic). The number of NFETs connected in series in any discharging path from any (internal) output to the ground should be less than or equal to 4. Available input: $x_1, \ldots, x_7, clock, \overline{clock}$. Ignore charge sharing. Try to minimize # TRs in your design. (10 points)



(2) Now, each internal node in your design has a parasitic capacitance c between the node and the ground (so all the internal nodes have the same parasitic capacitance). The output node has a capacitance C_{out} between the node and the ground.

Compute the energy consumption of your design for a single clock cycle (CLK switches from 0 to 1, and then 1 back to 0) and the input vector $x_1x_2 \ldots x_7 = 1110000$. (5 points)

During pre-charging, we charge/discharge some internal nodes. $0.5(8c + C_{out}){V_{DD}}^2$

During evaluation, we charge/discharge some nodes. $0.5(5c){V_{DD}}^2$

Total $0.5(13c + C_{out}){V_{DD}}^2$

(3) Repeat the computation of the energy consumption for the input vector $x_1x_2 \ldots x_7 = 1111100$. (5 points)

During pre-charging, we charge/discharge some internal nodes. $0.5(8c + C_{out}){V_{DD}}^2$

During evaluation, we charge/discharge some nodes. $0.5(7c){V_{DD}}^2$

Total $0.5(15c + C_{out}){V_{DD}}^2$

(4) Repeat the computation of the energy consumption for the input vector $x_1x_2 \ldots x_7 = 1111111$. (5 points)

During pre-charging, we charge/discharge some internal nodes. $0.5(8c + C_{out})V_{DD}{}^2$

During evaluation, we charge/discharge some nodes. $0.5(8c + C_{out})V_{DD}{}^2$

Total $0.5(16c + 2C_{out})V_{DD}{}^2$

(5) It is known that the input vector is $x_1x_2 \ldots x_7 = 1010101$ most of the time. Re-design the domino-logic-based 7-input AND gate so that you can minimize the energy consumption. (Notice that the design you made for Problem (1) might already be minimizing the energy consumption. In this case, you can just say that your design in (1) minimizes the energy consumption.) (5 points)