# EE466

# VLSI System Design

## Final Exam

## Dec. 11, 2023. (4:30pm – 6:30pm)

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**Name:**

**WSU ID:**

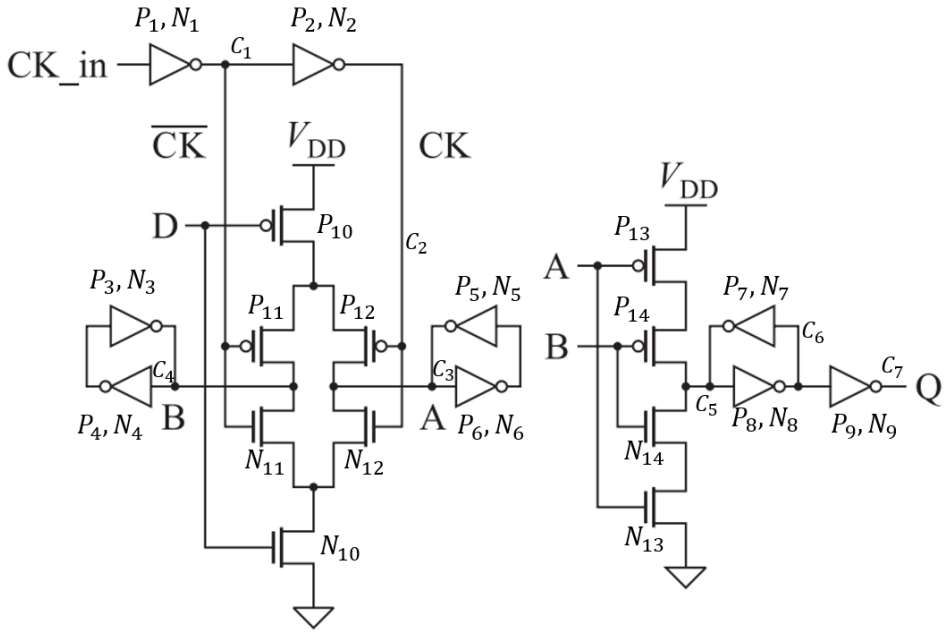
| Problem | Points | |
|---|---|---|
| 1 | 80 | |
| 2 | 20 | |
| 3 | 50 | |
| 4 | 20 | |
| 5 | 30 | |
| Total | 200 | |

* Allowed: Textbooks, cheat sheets, class notes, notebooks, calculators, watches

* Not allowed: Electronic devices (smart phones, tablet PCs, laptops, etc.) except calculators and watches

## Problem #1 (DFF, 80 points)

The following schematic shows a dual-edge D flip flop. Answer the following questions. Assume that all the setup and hold times are positive (≥0). You can also assume that $T_{CLK}$ is the clock period and the duty cycle is 50% (i.e., the clock is high for $\frac{T_{CLK}}{2}$ and low for $\frac{T_{CLK}}{2}$.) Use $C_1$ to $C_7$ for the capacitances of the nets shown in the figure. If a net does not have $C_{\#}$, then you can ignore the capacitance of the net. Use $R_{N\#}$ (or $R_{P\#}$) for the resistance of the NFET N# (or PFET P#). For example, $R_{N1}$ is the resistance of $N_1$.




Note: When node A, B, $C_5$, and $C_6$ are charged/discharged, you can ignore the impact of the cross-coupled inverters ($P_3, N_3, P_5, N_5, P_7, N_7$) on the delay/setup time/hold time/energy consumption calculation.

(1) Estimate the fall delay of the FF for $CLK = \nearrow$. (10 points)

(2) Estimate the rise delay of the FF for $CLK = \nearrow$. (10 points)

(3) Estimate the setup time of the FF for $D = 0$ and $CLK = \nearrow$. (10 points)

(4) Estimate the setup time of the FF for $D = 1$ and $CLK = \nearrow$. (10 points)

(5) Estimate the hold time of the FF for $D = 0$ and $CLK = \nearrow$. (10 points)

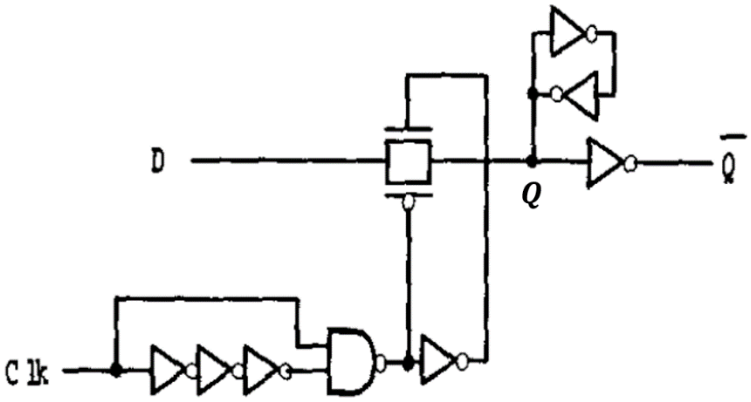
(6) Estimate the hold time of the FF for $D = 1$ and $CLK = \nearrow$. (10 points)

(7) Estimate the energy consumption of the FF for $D = 0$ and $CLK = \nearrow$. (10 points)

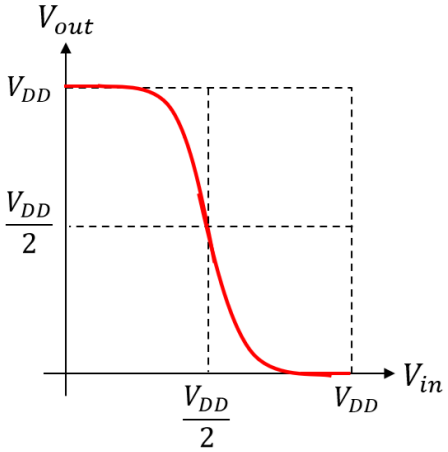
(8) Estimate the energy consumption of the FF for $D = 1$ and $CLK = \nearrow$. (10 points)

## Problem #2 (DC Analysis, 20 points)

The following shows an explicitly-pulsed hybrid static flip-flop (ep-SFF) design.

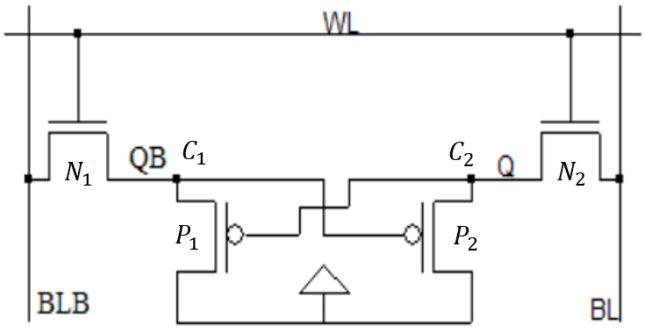



The following shows the DC characteristics of all the inverters in the figure.




Draw a DC characteristic curve (Q vs. D) for the above DFF.

## Problem #3 (Memory, 50 points)




The figure above shows a 4T SRAM cell (WL: Word line, BL: Bit line, BLB: Inverted bit line). When we write a logic value 1 to the cell, we set $BL$ to $V_{DD}$ and $\overline{BL}$ to 0V. Similarly, when we write a logic value 0 to the cell, we set $BL$ and $\overline{BL}$ to 0V and $V_{DD}$, respectively. (The triangle denotes VDD).

- Threshold voltage of an NFET (or PFET): $V_{tn}$ (or $V_{tp}$).
- ON resistance of NFET $N_{\#}$ (or PFET $P_{\#}$): $R_{n\#}$ (or $R_{p\#}$).
- Capacitance of a net: $C_{\#}$ (shown above).
- Assume $V_{tn} > |V_{tp}|$

(1) Show an inequality to be able to write a logical value 1 to the cell. (10 points)

(2) Show an inequality to be able to write a logical value 0 to the cell. (10 points)

(3) Suppose the cell has a logical value 0. We write a logical value 1 to the cell and then write a logical value 0 to the cell. Estimate the total energy consumption (use $C_1$ and $C_2$). (10 points)

Answer the following questions. Correct: +5 points, Wrong: -5 points, No answer: 0 points, Min: 0 points. You can ignore the parasitic capacitances of the transistors.

(4) If we increase the width of $P_1$, the delay for writing 1 to the cell goes down. (True / False)

(5) If we increase the width of $N_1$, the delay for writing 1 to the cell goes down. (True / False)

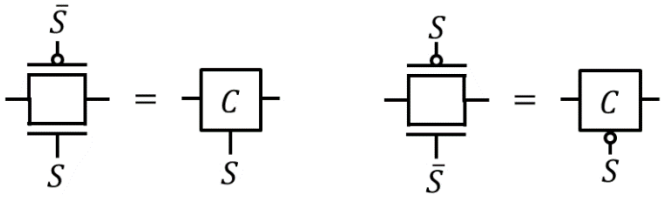
(6) If we increase the width of $P_2$, the delay for writing 1 to the cell goes down. (True / False)

(7) If we increase the width of $N_2$, the delay for writing 1 to the cell goes down. (True / False)

## Problem #4 (Logic Design, 20 points)

(1) Design $Y = A + B \cdot (C + D \cdot E \cdot F)$. Available input: $A, B, C, D, E, F$. Use the static CMOS design methodology (draw a schematic). (10 points)

(2) Design $Y$ using transmission gates. Available inputs: $A, B, C, D, E, F$ (and 0 and 1). Use the following symbols for the transmission gates. (10 points)




≤10 TGs: 10 points. ≤12 TGs: 8 points. ≤14 TGs: 6 points. Otherwise: 5 points.

## Problem #5 (Domino Logic, 30 points)

(1) Design a domino-logic-based 7-input AND gate, $Y = x_1 \cdot x_2 \cdot \ldots \cdot x_7$ (draw a schematic). The number of NFETs connected in series in any discharging path from any (internal) output to the ground should be less than or equal to 4. Available input: $x_1, \ldots, x_7, clock, \overline{clock}$. Ignore charge sharing. Try to minimize # TRs in your design. (10 points)

(2) Now, each internal node in your design has a parasitic capacitance $c$ between the node and the ground (so all the internal nodes have the same parasitic capacitance). The output node has a capacitance $C_{out}$ between the node and the ground.

Compute the energy consumption of your design for a single clock cycle (CLK switches from 0 to 1, and then 1 back to 0) and the input vector $x_1 x_2 \ldots x_7 = 1110000$. (5 points)

(3) Repeat the computation of the energy consumption for the input vector $x_1 x_2 \ldots x_7 = 1111100$. (5 points)

(4) Repeat the computation of the energy consumption for the input vector $x_1x_2 \ldots x_7 = 1111111$. (5 points)

(5) It is known that the input vector is $x_1x_2 \ldots x_7 = 1010101$ most of the time. Re-design the domino-logic-based 7-input AND gate so that you can minimize the energy consumption. (Notice that the design you made for Problem (1) might already be minimizing the energy consumption. In this case, you can just say that your design in (1) minimizes the energy consumption.) (5 points)