EE466

VLSI System Design

Final Exam

Oct. 17, 2024. (4:20pm – 5:35pm)

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Name:

WSU ID:

Problem	Points	
1	110	
2	10	
3	100	
Total	220	

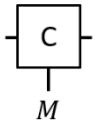
* Allowed: Textbooks, cheat sheets, class notes, notebooks, calculators, watches

* Not allowed: Electronic devices (smart phones, tablet PCs, laptops, etc.) except calculators and watches

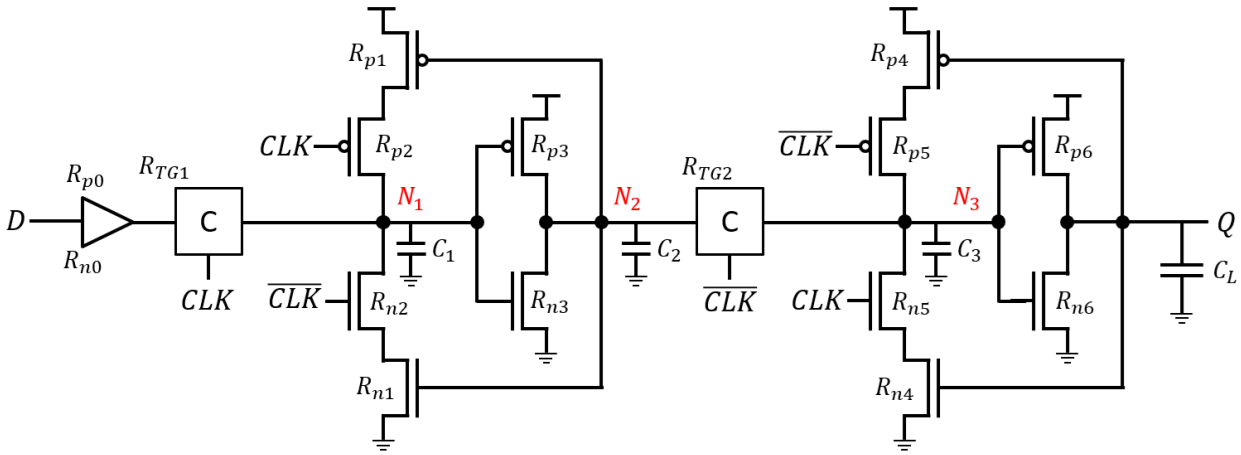
Problem #1 (DFF, 110 points)

The following schematic shows a D flip flop. Answer the following questions.

- Assume that all the setup and hold times are positive (≥0).
- If a net (node) does not have $C_{\#}$, then you can ignore its capacitance.
- Use $R_{\#}$ for the resistance of the corresponding NFET, PFET, or TG.



- is a transmission gate (TG) and turned on when M is high (1).
- For the input buffer, you can think of it as a circuit having a PFET network (whose resistance is R_{p0}) and an NFET network (resistance: R_{n0}).



(1) Is it positive-edge-triggered or negative-edge-triggered? (10 points)

When CLK=1, $N_1 = D$ and $N_2 = \overline{D}$. When CLK goes low, TG2 is turned on and $N_3 = N_2 = \overline{D}$, so $Q = D$. Thus, this is a negative-edge-triggered D FF.

(2) Estimate the fall delay of the FF. (10 points)

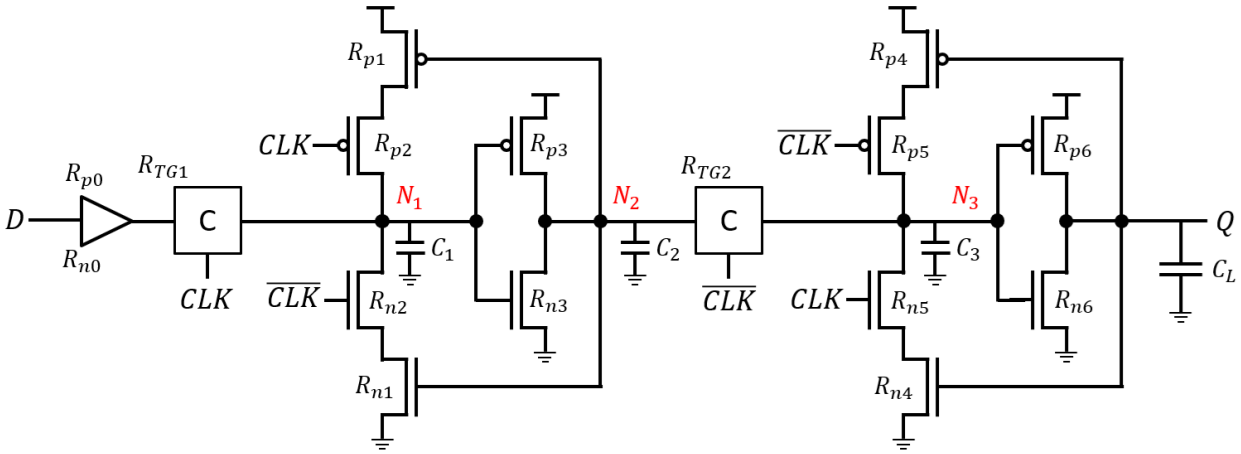
Suppose D=0, Q=1, and CLK=1. $N_1 = 0$. $N_2 = 1$. $N_3 = 0$. When CLK goes low, TG2 is turned on and N_3 is pulled up by R_{p3} (delay = $(R_{p3} + R_{TG2}) \cdot C_3$). Then, Q is discharged by R_{n6} (delay = $R_{n6} \cdot C_L$).

Answer: $(R_{p3} + R_{TG2}) \cdot C_3 + R_{n6} \cdot C_L$.

(3) Estimate the rise delay of the FF. (10 points)

D=1, Q=0, CLK=1. $N_1 = 1$. $N_2 = 0$. $N_3 = 1$. When CLK goes low, TG2 is turned on and N_3 is discharged by R_{n3} (delay = $(R_{n3} + R_{TG2}) \cdot C_3$). Then, Q is charged by R_{p6} (delay = $R_{p6} \cdot C_L$).

Answer: $(R_{n3} + R_{TG2}) \cdot C_3 + R_{p6} \cdot C_L$.



(4) Estimate the setup time of the FF for $D = 0$. (10 points)

D=1, Q=1, CLK=1. $N_1 = 1, N_2 = 0, N_3 = 0$. If D becomes 0, then $N_1 = 0$, then $N_2 = 1$. CLK can go low only after $N_2 = 1$. The discharging time for N_1 is $(R_{n0} + R_{TG1}) \cdot C_1$. The charging time for N_2 is $R_{p3} \cdot C_2$.

Answer: $(R_{n0} + R_{TG1}) \cdot C_1 + R_{p3} \cdot C_2$.

(5) Estimate the setup time of the FF for $D = 1$. (10 points)

D=0, Q=0, CLK=1. $N_1 = 0, N_2 = 1, N_3 = 1$. If D becomes 1, then $N_1 = 1$, then $N_2 = 0$. CLK can go low only after $N_2 = 0$. The charging time for N_1 is $\left(R_{p0} + R_{TG1}\right) \cdot C_1$. The discharging time for N_2 is $R_{n3} \cdot C_2$.

Answer: $\left(R_{p0} + R_{TG1}\right) \cdot C_1 + R_{n3} \cdot C_2$.

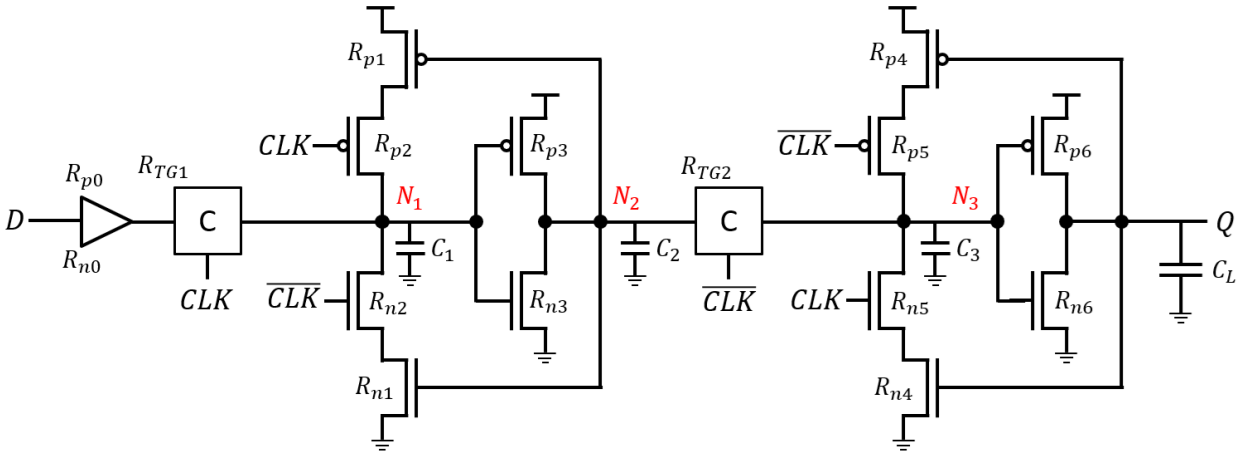
(6) Estimate the hold time of the FF for $D = 0$. (10 points)

D=0, Q=1, CLK=1. $N_1 = 0, N_2 = 1, N_3 = 0$. If CLK goes low, then TG1 is turned off. Then, even if D changes, Q is not affected by that. Thus, the hold time is zero (or just to be safe, some small value.)

Answer: 0 or delta.

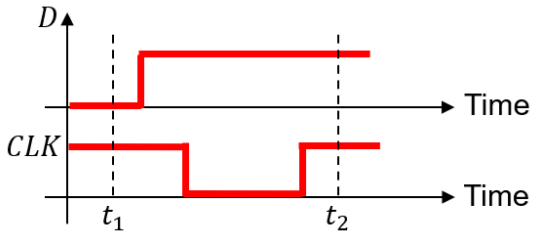
(7) Estimate the hold time of the FF for $D = 1$. (10 points)

Answer: 0 or delta (for the same reason as in (6)).



(8) Estimate the followings. Assume that Q=0 at time t_1. (20 points)

a) Energy delivered from the DC source to the FF between t_1 and t_2.
b) Energy dissipated in the FF between t_1 and t_2.



D=0, Q=0. $N_1 = 0$, $N_2 = 1$, $N_3 = 1$.

First, D goes high, so N_1 is charged and N_2 is discharged.

When CLK goes low, N_3 is discharged and Q is charged.

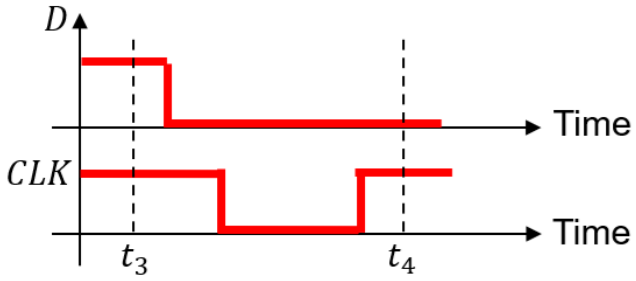
When CLK goes high, nothing happens.

Answer:

a) Energy delivered from the DC source to the FF: $(C_1 + C_L) \cdot {V_{DD}}^2$.
b) Energy dissipated in the FF: $\frac{1}{2}(C_1 + C_2 + C_3 + C_L) \cdot {V_{DD}}^2$

(9) Estimate the followings. Assume that Q=1 at time t_3. (20 points)

a) Energy delivered from the DC source to the FF between t_3 and t_4.
b) Energy dissipated in the FF between t_3 and t_4.



D=1, Q=1. $N_1 = 1, N_2 = 0,\ N_3 = 0$.

First, D goes low, so N_1 is discharged and N_2 is charged.

When CLK goes low, N_3 is charged and Q is discharged.

When CLK goes high, nothing happens.

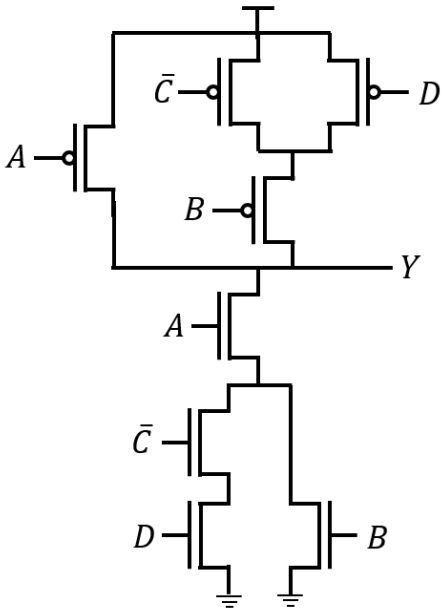
Answer:

a) Energy delivered from the DC source to the FF: $(C_2 + C_3) \cdot {V_{DD}}^2$.
b) Energy dissipated in the FF: $\frac{1}{2}(C_1 + C_2 + C_3 + C_L) \cdot {V_{DD}}^2$

Problem #2 (Logic Design, 10 points)

Design $Y = \bar{A} + \bar{B} \cdot (C + \bar{D})$. Available input: A, B, C, D. Use the static CMOS design methodology (draw a schematic). (10 points)

$$Y = \overline{A \cdot \{B + \bar{C} \cdot D\}}$$

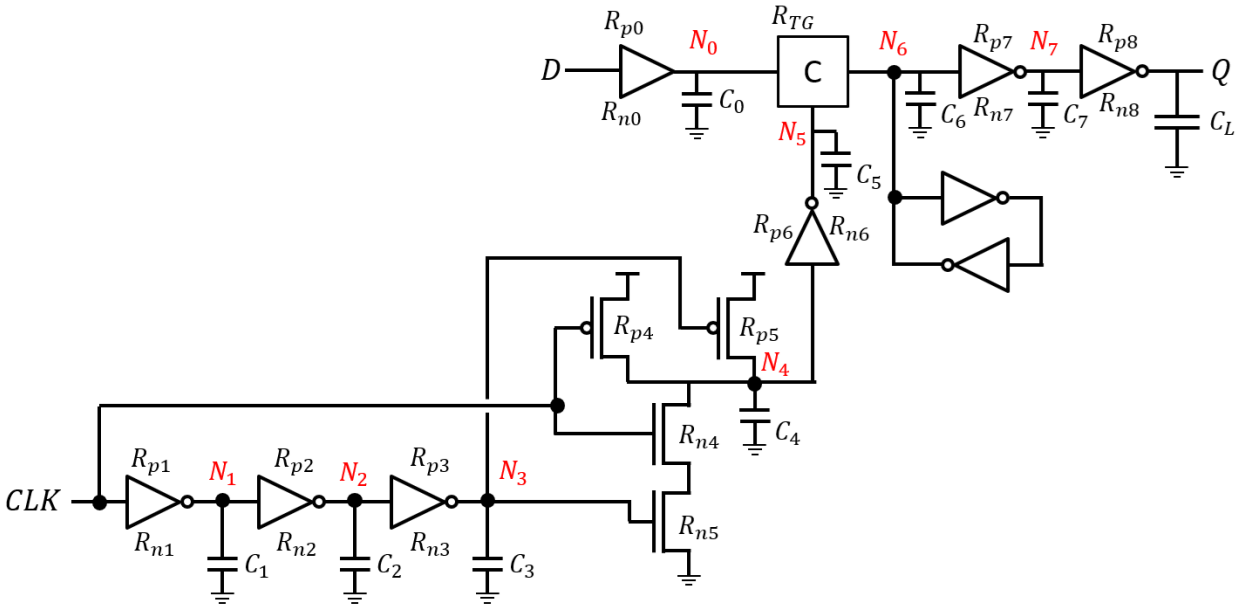


Problem #3 (DFF, 100 points)

The following schematic shows a positive-edge-triggered D flip flop. Answer the following questions.

- Assume that all the setup and hold times are positive (≥0).
- If a net (node) does not have $C_{\#}$, then you can ignore its capacitance.
- Use $R_{\#}$ for the resistance of the corresponding NFET, PFET, or TG.

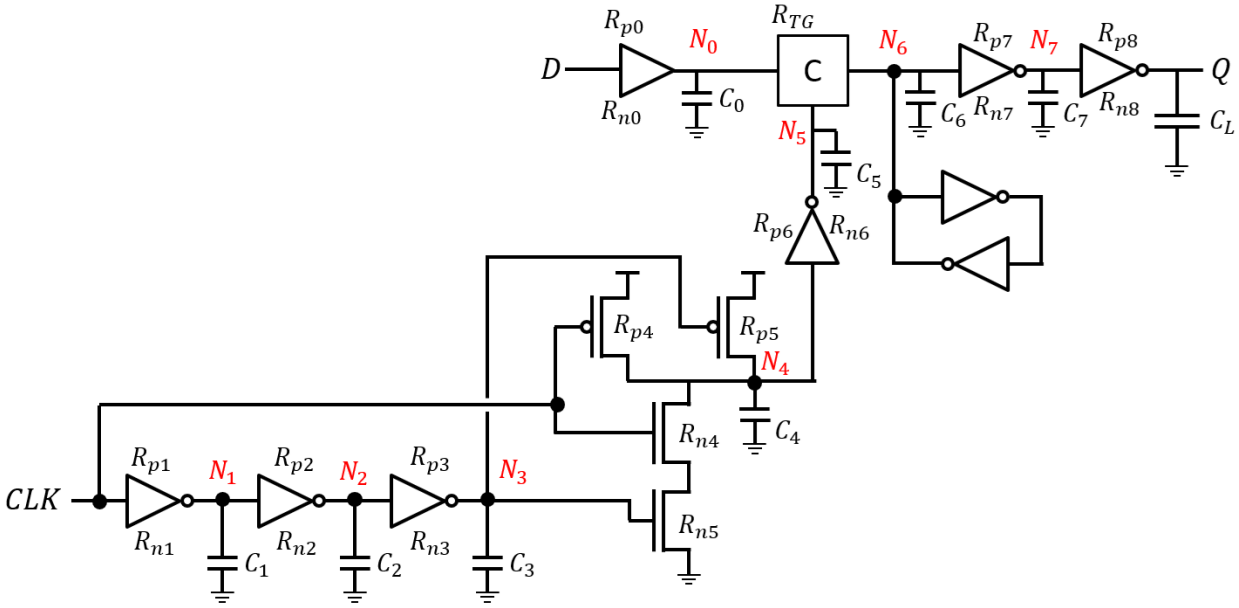
- is a transmission gate (TG) and turned on when M is high (1).
- For the input buffer, you can think of it as a circuit having a PFET network (whose resistance is R_{p0}) and an NFET network (resistance: R_{n0}).
- When you analyze the delay/setup/hold times, ignore the R and C of the cross-coupled inverters.



(1) Estimate the fall delay of the FF. (10 points)

Suppose D=0, Q=1, and CLK=0. $N_1 = 1$. $N_2 = 0$. $N_3 = 1$. When CLK goes high, N_4 is discharged and $N_5 = 1$, so the TG is turned on. Then, N_6 is discharged, N_7 is charged, and Q is discharged.

Answer: $(R_{n4} + R_{n5})C_4 + R_{p6} \cdot C_5 + (R_{n0} + R_{TG})C_6 + R_{p7} \cdot C_7 + R_{n8} \cdot C_L$.



(2) Estimate the rise delay of the FF. (10 points)

Suppose D=1, Q=0, and CLK=0. $N_1 = 1$. $N_2 = 0$. $N_3 = 1$. When CLK goes high, N_4 is discharged and $N_5 = 1$, so the TG is turned on. Then, N_6 is charged, N_7 is discharged, and Q is charged.

Answer: $(R_{n4} + R_{n5})C_4 + R_{p6} \cdot C_5 + (R_{p0} + R_{TG})C_6 + R_{n7} \cdot C_7 + R_{p8} \cdot C_L$.

(3) Estimate the setup time of the FF for $D = 0$. (10 points)

Suppose D=1, Q=1, and CLK=0. $N_1 = 1$. $N_2 = 0$. $N_3 = 1$. When CLK goes high, N_4 is discharged and $N_5 = 1$, so the TG is turned on. N_0 must be 0 before the TG is turned on (otherwise it might not be possible to discharge N_6 in time). Discharging N_0 takes $R_{n0}C_0$. If this is shorter than the time taken to turn on the TG, then the setup time is 0. However, if it is longer than the time taken to turn on the TG, the difference between the two is the setup time.

Answer: Max (0, $R_{n0} \cdot C_0 - (R_{n4} + R_{n5})C_4 + R_{p6} \cdot C_5$).

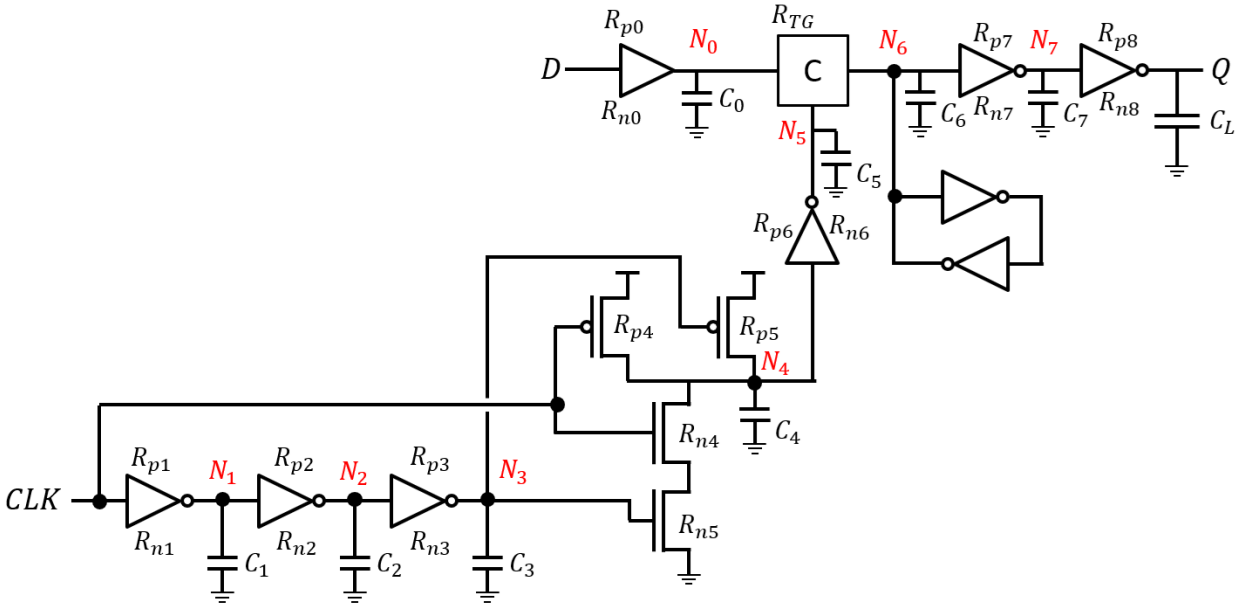
(4) Estimate the setup time of the FF for $D = 1$. (10 points)

Answer: Max (0, $R_{p0} \cdot C_0 - (R_{n4} + R_{n5})C_4 + R_{p6} \cdot C_5$).

(5) Estimate the hold time of the FF for $D = 0$. (10 points)

D is allowed to change arbitrarily after the TG is turned off.

Answer: $R_{n1} \cdot C_1 + R_{p2} \cdot C_2 + R_{n3} \cdot C_3 + R_{p5} \cdot C_4 + R_{n6} \cdot C_5$

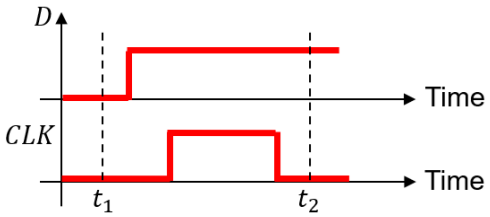


(6) Estimate the hold time of the FF for $D = 1$. (10 points)

Answer: $R_{n1} \cdot C_1 + R_{p2} \cdot C_2 + R_{n3} \cdot C_3 + R_{p5} \cdot C_4 + R_{n6} \cdot C_5$

(7) Estimate the followings. Assume that Q=0 at time t_1. (20 points)

c) Energy delivered from the DC source to the FF between t_1 and t_2.
d) Energy dissipated in the FF between t_1 and t_2.



D=0, Q=0. $N_1 = 1, N_2 = 0,\ N_3 = 1, N_4 = 1, N_5 = 0, N_0 = 0, N_6 = 0, N_7 = 1.$

First, D goes high, so N_0 is charged.

When CLK goes high, N_4 is discharged, N_5 is charged, N_6 is charged, N_7 is discharged, and Q is charged. At the same time, N_1 is discharged, N_2 is charged, and N_3 is discharged, so N_4 is charged, N_5 is discharged.

When CLK goes low, $N_1 = 1$, $N_2 = 0$, and $N_3 = 1$.

Answer:

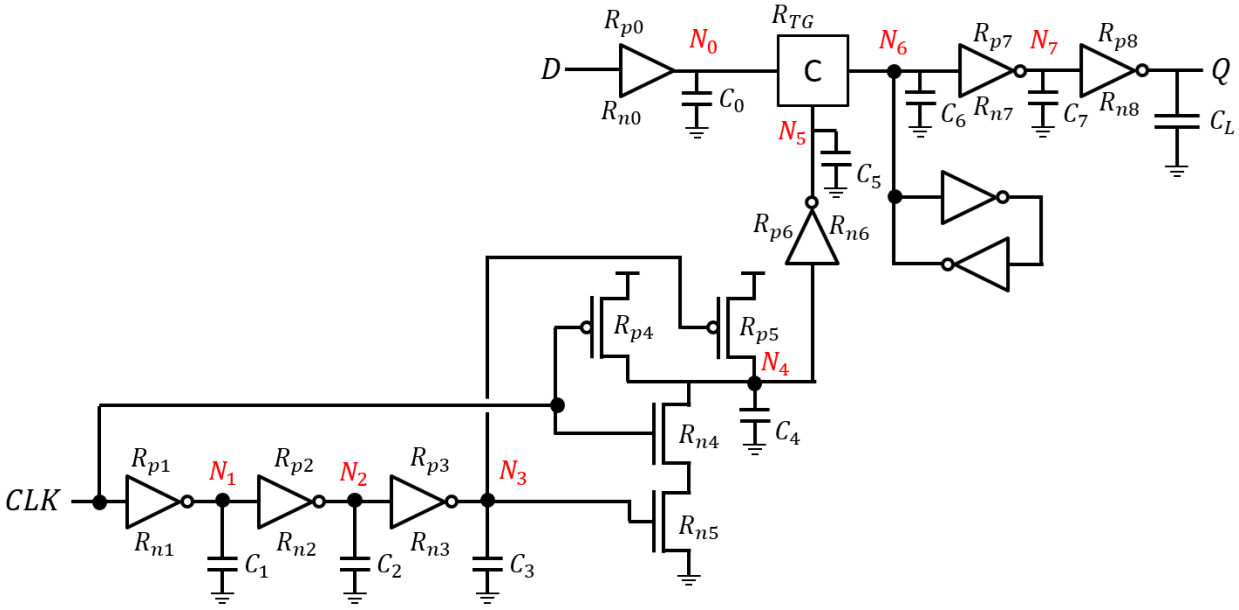
a) Energy delivered from the DC source to the FF:

$(C_0 + C_5 + C_6 + C_L + C_2 + C_4 + C_1 + C_3) \cdot {V_{DD}}^2 = (C_0 + C_1 + C_2 + C_3 + C_4 + C_5 + C_6 + C_L) \cdot {V_{DD}}^2$.

b) Energy dissipated in the FF:

$$\frac{1}{2}(C_0 + C_4 + C_5 + C_6 + C_7 + C_L + C_1 + C_2 + C_3 + C_4 + C_5 + C_1 + C_2 + C_3) \cdot {V_{DD}}^2$$

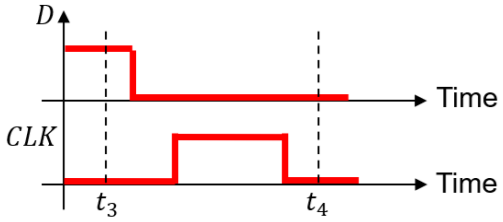
$$= \frac{1}{2}(C_0 + 2C_1 + 2C_2 + 2C_3 + 2C_4 + 2C_5 + C_6 + C_7 + C_L) \cdot {V_{DD}}^2$$



(8) Estimate the followings. Assume that Q=1 at time t_3. (20 points)

c) Energy delivered from the DC source to the FF between t_3 and t_4.

d) Energy dissipated in the FF between t_3 and t_4.



D=1, Q=1. $N_1 = 1, N_2 = 0, N_3 = 1, N_4 = 1, N_5 = 0, N_0 = 1, N_6 = 1, N_7 = 0$.

First, D goes low, so N_0 is discharged.

When CLK goes high, N_4 is discharged, N_5 is charged, N_6 is discharged, N_7 is charged, and Q is discharged. At the same time, N_1 is discharged, N_2 is charged, and N_3 is discharged, so N_4 is charged, N_5 is discharged.

When CLK goes low, $N_1 = 1$, $N_2 = 0$, and $N_3 = 1$.

Answer:

a) Energy delivered from the DC source to the FF:

$$(C_5 + C_7 + C_2 + C_4 + C_1 + C_3) \cdot {V_{DD}}^2 = (C_1 + C_2 + C_3 + C_4 + C_5 + C_7) \cdot {V_{DD}}^2.$$

b) Energy dissipated in the FF:

$$\frac{1}{2}(C_0 + C_4 + C_5 + C_6 + C_7 + C_L + C_1 + C_2 + C_3 + C_4 + C_5 + C_1 + C_2 + C_3) \cdot {V_{DD}}^2$$

$$= \frac{1}{2}(C_0 + 2C_1 + 2C_2 + 2C_3 + 2C_4 + 2C_5 + C_6 + C_7 + C_L) \cdot {V_{DD}}^2$$