EE466

VLSI System Design

Midterm Exam

Oct. 17, 2024. (4:20pm – 5:35pm)

Instructor: Dae Hyun Kim (daehyun.kim@wsu.edu)

Name:

WSU ID:

Problem	Points	
1	110	
2	10	
3	100	
Total	220	

* Allowed: Textbooks, cheat sheets, class notes, notebooks, calculators, watches

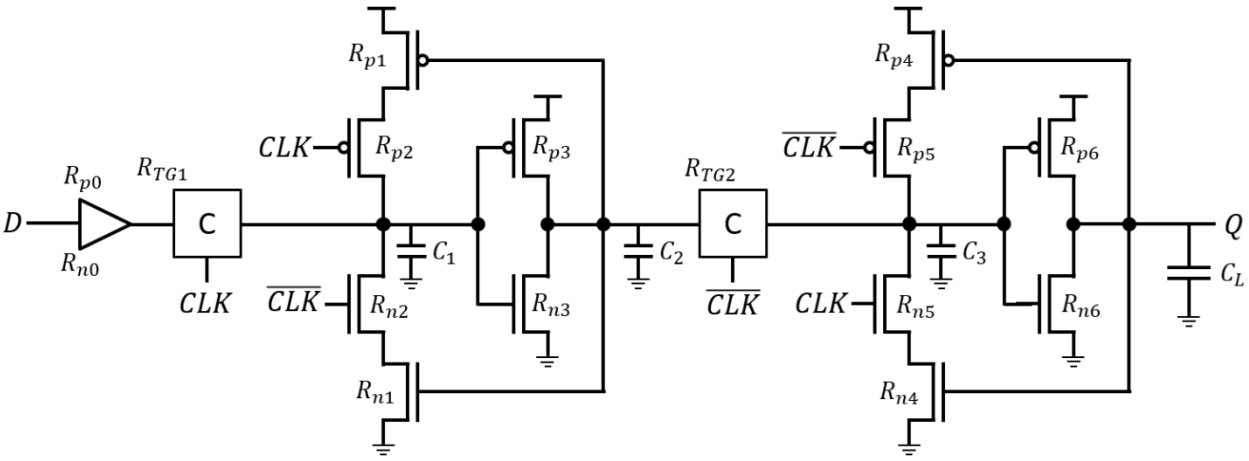
* Not allowed: Electronic devices (smart phones, tablet PCs, laptops, etc.) except calculators and watches

Problem #1 (DFF, 110 points)

The following schematic shows a D flip flop. Answer the following questions.

- Assume that all the setup and hold times are positive (≥0).
- If a net (node) does not have $C_{\#}$, then you can ignore its capacitance.
- Use $R_{\#}$ for the resistance of the corresponding NFET, PFET, or TG.

- M is a transmission gate (TG) and turned on when M is high (1).
- For the input buffer, you can think of it as a circuit having a PFET network (whose resistance is R_{p0}) and an NFET network (resistance: R_{n0}).

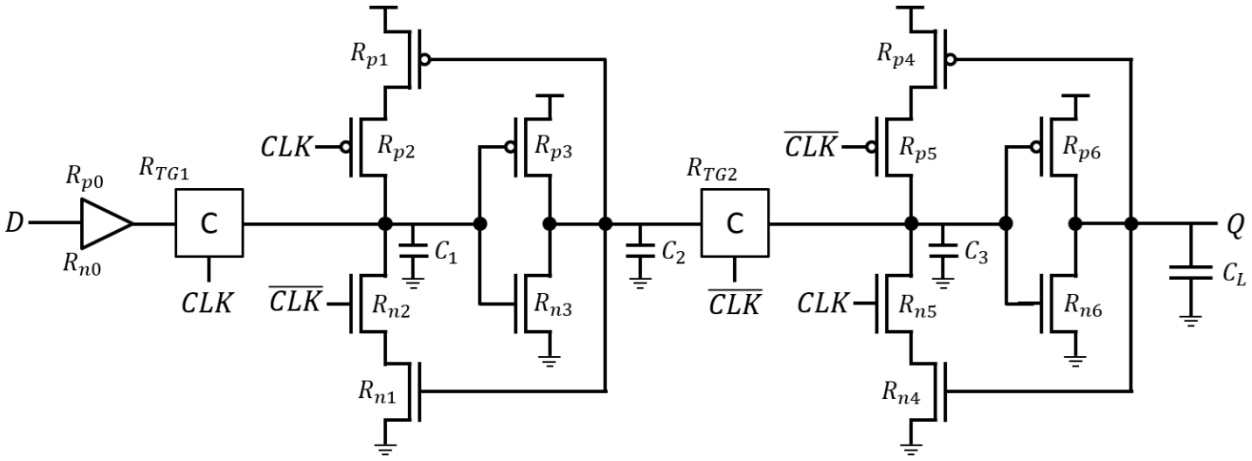


(1) Is it positive-edge-triggered or negative-edge-triggered? (10 points)

(If your answer is wrong, then you will get 0 points in Problem 1 because all the following questions are based on the polarity of the D FF.)

(2) Estimate the fall delay of the FF. (10 points)

(3) Estimate the rise delay of the FF. (10 points)

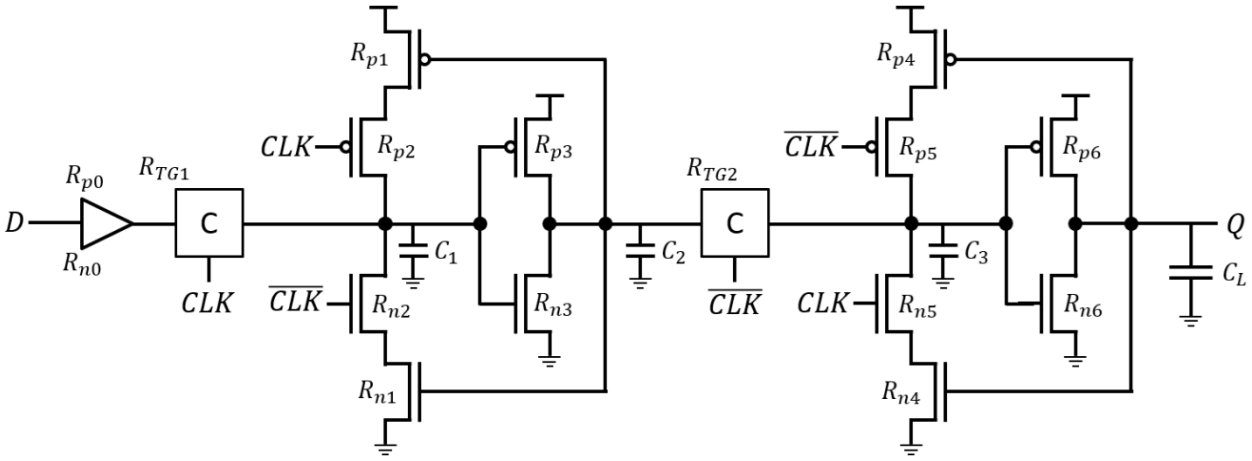


(4) Estimate the setup time of the FF for $D = 0$. (10 points)

(5) Estimate the setup time of the FF for $D = 1$. (10 points)

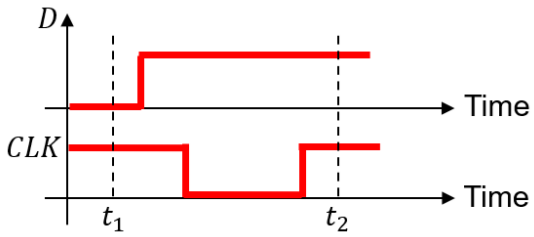
(6) Estimate the hold time of the FF for $D = 0$. (10 points)

(7) Estimate the hold time of the FF for $D = 1$. (10 points)



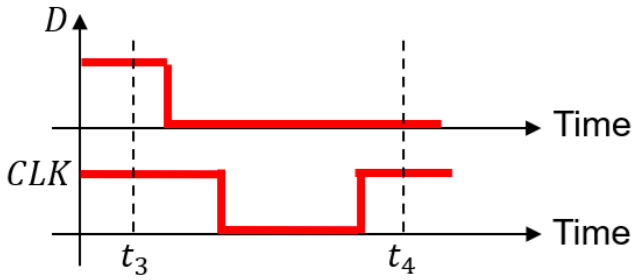
(8) Estimate the followings. Assume that Q=0 at time t_1. (20 points)

a) Energy delivered from the DC source to the FF between t_1 and t_2.
b) Energy dissipated in the FF between t_1 and t_2.



(9) Estimate the followings. Assume that Q=1 at time t_3. (20 points)

a) Energy delivered from the DC source to the FF between t_3 and t_4.
b) Energy dissipated in the FF between t_3 and t_4.



Problem #2 (Logic Design, 10 points)

Design $Y = \bar{A} + \bar{B} \cdot (C + \overline{D})$. Available input: A, B, C, D. Use the static CMOS design methodology (draw a schematic). (10 points)

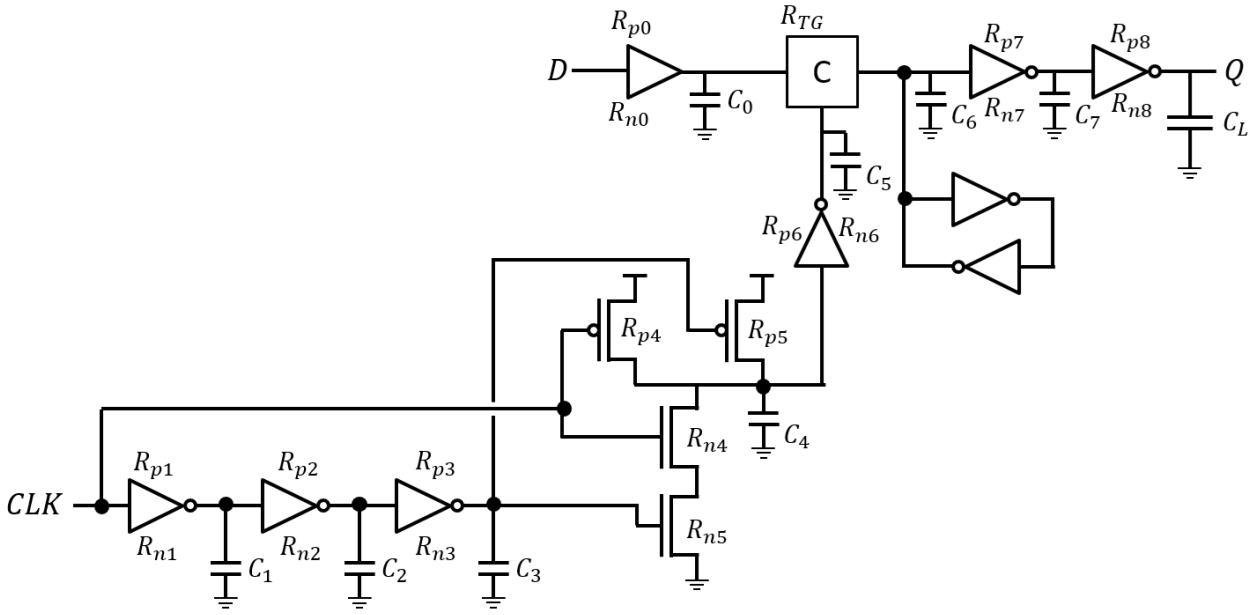
TRs <=10: 10 points, <= 12: 7 points, <=14: 5 points, >=15: 3 points

Problem #3 (DFF, 100 points)

The following schematic shows a positive-edge-triggered D flip flop. Answer the following questions.

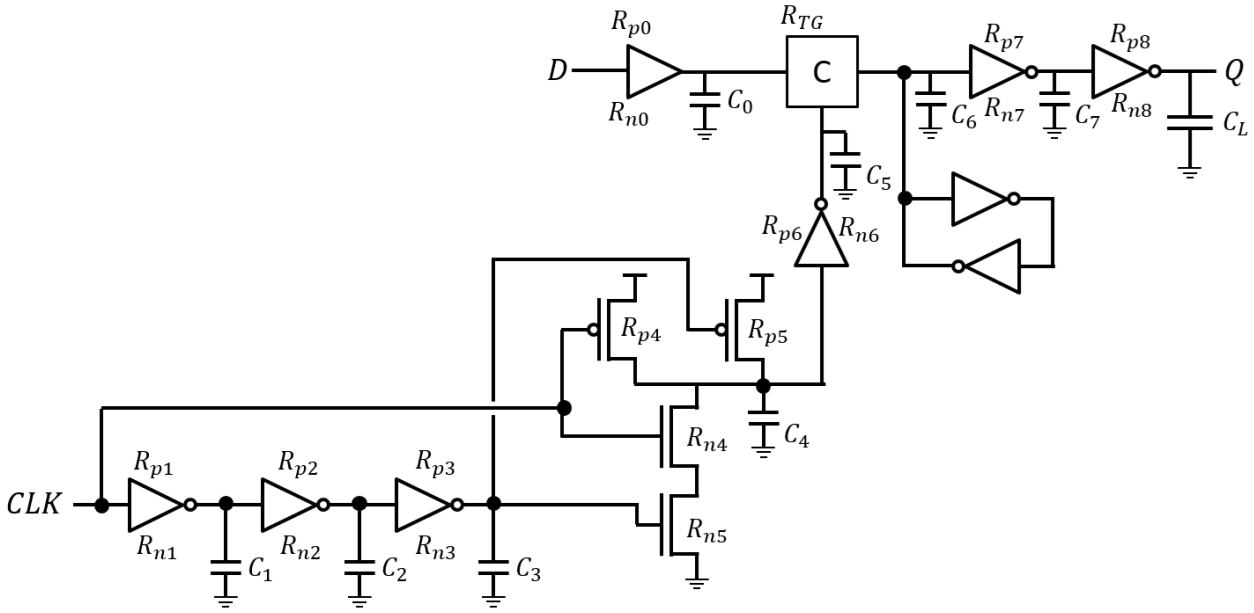
- Assume that all the setup and hold times are positive (≥0).
- If a net (node) does not have $C_{\#}$, then you can ignore its capacitance.
- Use $R_{\#}$ for the resistance of the corresponding NFET, PFET, or TG.

- is a transmission gate (TG) and turned on when M is high (1).
- For the input buffer, you can think of it as a circuit having a PFET network (whose resistance is R_{p0}) and an NFET network (resistance: R_{n0}).
- When you analyze the delay/setup/hold times, ignore the R and C of the cross-coupled inverters.



(1) Estimate the fall delay of the FF. (10 points)

(2) Estimate the rise delay of the FF. (10 points)

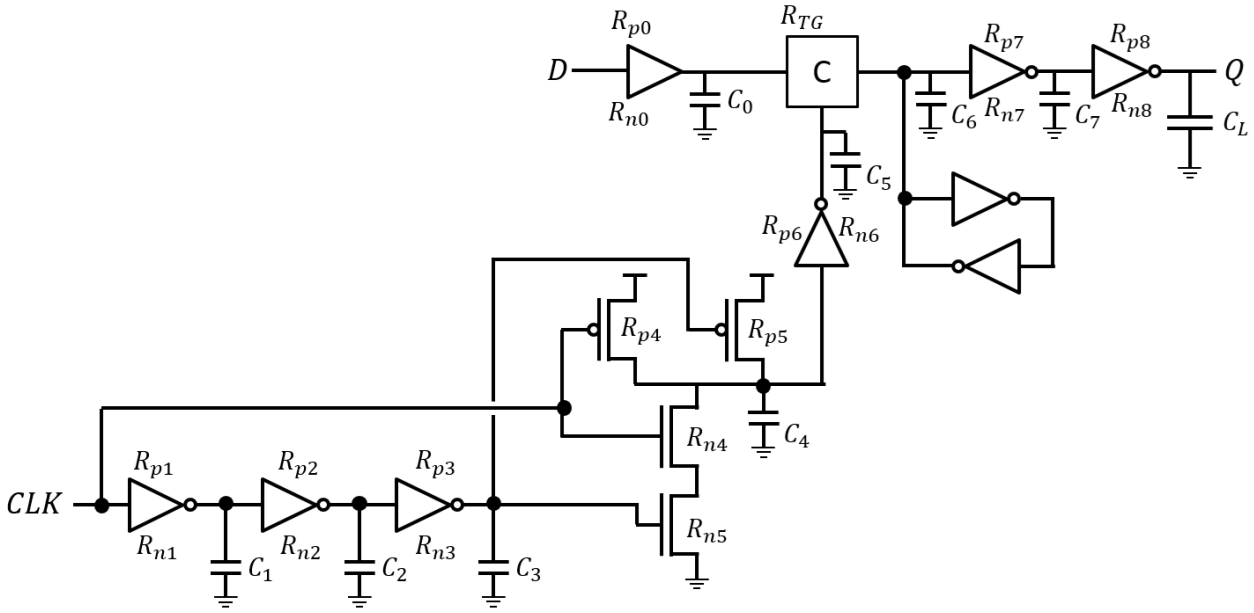


(3) Estimate the setup time of the FF for $D = 0$. (10 points)

(4) Estimate the setup time of the FF for $D = 1$. (10 points)

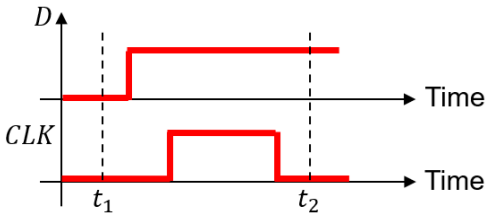
(5) Estimate the hold time of the FF for $D = 0$. (10 points)

(6) Estimate the hold time of the FF for $D = 1$. (10 points)



(7) Estimate the followings. Assume that Q=0 at time t_1. (20 points)

c) Energy delivered from the DC source to the FF between t_1 and t_2.
d) Energy dissipated in the FF between t_1 and t_2.



(8) Estimate the followings. Assume that Q=1 at time t_3. (20 points)

c) Energy delivered from the DC source to the FF between t_3 and t_4.
d) Energy dissipated in the FF between t_3 and t_4.