Suppose R\# is an 8-bit register. The data stored in R\# is treated as an unsigned binary number. We want to calculate the following for given input $R_{1}$ ( $\%$ is the MOD operation):

$$
\begin{gathered}
R_{2}=2 \cdot R_{1} \text { if } R_{1} \leq 127 \\
R_{2}=2 \cdot\left(R_{1}-128\right) \text { if } R_{1} \geq 128
\end{gathered}
$$

$R_{1}$ is stored in register R 1 (input) and $R_{2}$ is the result that will be stored in register R 2 . The above function can be implemented by two assembly instructions with two constants C1 and C2 as follows:
$\square$ R2, R1, \#C1
$\square$ R2, R2, \#C2

Find the instructions and the constants. Notice that the instructions must be the ones shown in the instruction page.

Suppose $R_{1}=x_{7} x_{6} \ldots x_{0}$. If $R_{1} \leq 127, x_{7}$ is 0 , so $R_{2}$ is just $2 \cdot R_{1}$.
However, if $R_{1} \geq 128$ (i.e., $x_{7}=1$ ), we should subtract 128 from $R_{1}$, which is setting
$x_{7}$ to 0 . Thus, $x_{7}$ should always be set to zero $=>$ masking. Thus, the first instruction is AND R2, R1, \#0x7F.
Now, we multiply it by 2 . It can be "MUL R2, R2, \#2" or "LSL R2, R2, \#1".

Suppose R\# is an 8-bit register. The data stored in R\# is treated as an unsigned binary number. We want to calculate the following for given input $R_{1}$ ( $\%$ is the MOD operation):

$$
R_{2}=85-R_{1}+
$$

$$
2 *\left[\left\{\left(R_{1} \% 256\right)+\left(R_{1} \% 64\right)+\left(R_{1} \% 16\right)+\left(R_{1} \% 4\right)\right\}-\left\{\left(R_{1} \% 128\right)+\left(R_{1} \% 32\right)+\left(R_{1} \% 8\right)+\left(R_{1} \% 2\right)\right\}\right]
$$

$R_{1}$ is stored in register R1 (input) and $R_{2}$ is the result that will be stored in register R2. The above function can be implemented by one assembly instruction with a constant C as follows:

> R2, R1, \#C1

Find the instruction and the constant. (Don't care about overflows.)
Suppose $R_{1}=x_{7} x_{6} \ldots x_{0} .85$ is 01010101 in binary form.
( $R_{1} \% 256$ ) is just $x_{7} x_{6} \ldots x_{0}$. ( $R_{1} \% 64$ ) is $00 x_{5} x_{4} \ldots x_{0}$. ( $R_{1} \% 16$ ) is $0000 x_{3} x_{2} x_{1} x_{0}$. Thus, $\left[\left\{\left(R_{1} \% 256\right)+\ldots+\left(R_{1} \% 4\right)\right\}-\left\{\left(R_{1} \% 128\right)+\cdots+\left(R_{1} \% 2\right)\right\}\right]$ is $x_{7} 0 x_{5} 0 x_{3} 0 x_{1} 0$.

$$
R_{2}+R_{1}=2 *\left(x_{7} 0 x_{5} 0 x_{3} 0 x_{1} 0\right)+01010101
$$

Suppose $R_{2}=y_{7} y_{6} \ldots y_{0}$. Then,

$$
\begin{aligned}
& \begin{array}{l}
y_{7} y_{6} y_{5} y_{4} y_{3} y_{2} y_{1} y_{0} \\
+ \\
x_{7} x_{6} x_{5} x_{4} x_{3} x_{2} x_{1} x_{0}
\end{array} \\
& x_{7} 0 x_{5} 0 x_{3} 0 x_{1} 0
\end{aligned} \longrightarrow \frac{\begin{array}{l}
y_{7} y_{6} y_{5} y_{4} y_{3} y_{2} y_{1} y_{0} \\
+0 x_{6} 0 x_{4} 0 x_{2} 0 x_{0}
\end{array}}{x_{7} 1 x_{5} 1 x_{3} 1 x_{1} 1}
$$

Thus, $R_{2}=x_{7} \overline{x_{6}} x_{5} \overline{x_{4}} x_{3} \overline{x_{2}} x_{1} \overline{x_{0}}$.
Answer: EOR (XOR) R2, R1, \#85 // 85 is 01010101

Now, let's use the 32-bit ARM architecture, i.e., R\# is a 32-bit register and int is a 32-bit signed integer. How will the main memory look like after the following code is executed? Draw a figure for the main memory.

$$
\begin{aligned}
& \text { int } x[8] \text {; } \\
& \text { for ( int } i=0 ; i<8 ; i++ \text { ) } \\
& x[i]=i ;
\end{aligned}
$$

I just randomly chose 0x6000 for the starting address. It doesn't matter what number you choose for that, but it should be an integer multiple of 4.


Use the 32-bit ARM architecture. Write an assembly code for the following C code. The starting address of array x is $0 \times 5000$.

$$
\begin{aligned}
& \text { int } x[8] \text {; } \\
& \text { for ( int } i=0 ; i<8 ; i++) \\
& x[i]=i ;
\end{aligned}
$$

LDR R1, =\#0x5000
MOV R2, \#0 // i
loop:
STR R2, [R1] // x[i] = i
ADD R2, R2, \#1 // i++
ADD R1, R1, \#4 // the address for the next x[i]. It is increased by 4 (bytes).
CMP R2, \#8
BNE loop // if (i<8), go back to the loop
// done

* Notice that we cannot use something like STR R2, [R1, R3] for the offset. The instruction format is STR R\#, [R\#, \#imm] where \#imm is a constant. Thus, I am increasing R1 itself to access the next element.

Use the 32-bit ARM architecture.
int $x[4][8] ;$
The address of $x[0][0]$, i.e., $\&(x[0][0])$, is $0 x 6000$.
What is the address of $x[1][2]$ ?
The address of $\times[1][0]$ is $0 \times 6000+8 *(4$ bytes $)=0 \times 6000+32=0 \times 6020$.
Thus, the address of $x[1][2]$ is $0 \times 6020+2 *(4$ bytes $)=0 \times 6028$.
What is the address of $x[3][5]$ ?
The address of $x[3][0]$ is $0 \times 6000+8^{*}(4$ bytes $) * 3=0 \times 6000+96=0 \times 6060$.
Thus, the address of $x[3][5]$ is $0 \times 6060+5 *(4$ bytes $)=0 \times 6074$.

