EE 466
VLSI Design

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Course Website

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- Grading
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  - (send me your 5-letter code (all uppercase) by email)

Themes

- Arithmetic logic design
  - High-speed adders
  - High-speed multipliers
- VLSI (some overlaps with EE434)
  - Transistors, inverters, CMOS logic
  - Analysis: AC, DC, power, energy, leakage
  - Advanced design techniques (dynamic/domino/ratio-ed logic)
  - Logical efforts
  - Flip-flops
- Memory design
- FPGA architecture

- At the end of this semester, you will be able to
  - Understand high-speed arithmetic logic architectures
  - Design, analyze, and optimize CMOS logic and memory
  - Understand basic FPGA architectures

References

- N. Weste, “CMOS VLSI Design: A Circuits and Systems Perspective,” 4/E, 2010, Pearson, ISBN 978-0321547743

- J. Rabaey, “Digital Integrated Circuits,” 2/E, 2003, Pearson, ISBN 978-0130909961

- D. Hodges, “Analysis and Design of Digital Integrated Circuits,” 3/E, 2003, McGraw-Hill, ISBN 978-0072283655

- J. Uyemura, “CMOS Logic Circuit Design,” 2001E, 1999, Springer, ISBN 978-0792384526

Schedule

Week	Contents
1 (8/25, 27)	Introduction to VLSI, ASIC design, hardware algorithms, number systems
2 (9/1, 3)	Basic computer arithmetic, high-speed adders
3 (9/8, 10)	High-speed adders, redundant number systems
4 (9/15, 17)	High-speed adders, high-speed multipliers
5 (9/22, 24)	High-speed multipliers, transistors, inverter, CMOS logic
6 (9/29, 10/1)	Combinational CMOS logic design and analysis
7 (10/6, 8)	Midterm 1, combinational CMOS logic design and analysis
8 (10/13, 15)	Sequential CMOS logic design and analysis, project description
9 (10/20, 22)	Sequential CMOS logic design and analysis
10 (10/27, 29)	Advanced CMOS design techniques
11 (11/3, 5)	Advanced CMOS design techniques
12 (11/10, 12)	Midterm 2, Logical efforts
13 (11/17, 19)	Memory
14 (11/23 – 27)	Break
15 (12/1, 3)	Memory, FPGA architecture
16 (12/8, 10)	FPGA architecture, VLSI design, project due
Dec. 14	Final exam (4pm – 7pm)

Grading

- Homework assignments: 20%
- Lab assignments: 20%
- Project: 20%
- Midterms 1, 2: 20% (10% each)
- Final: 20%

- All the exams are open-book (you can use whatever you want. Laptops, calculators, books, notes, PPTs, etc.)

Assignments

- Homework & lab assignments
  - Late submission penalty
    - -5%/day
    - maximum -50%

- Labs are very important parts of this course.
  - Lab assignments will include HSpice simulations and Design Compiler netlist synthesis and analysis.
    - No worries! I will provide very detailed tutorials and manuals.
  - TAs will be available only during their office hours.