

EE 466/566**Catalog Description:**

Very Large Scale Integrated circuit, system and physical design using CAD software, project specification, modeling, implementation, documentation and reporting.

Semester: Fall 2020

Instructor: Dae Hyun Kim

Office: EME 504

Email: daehyun@eecs.wsu.edu

Phone: 509-335-3067

Office Hours: MWF 3:10 – 4pm (zoom) or by appointment

TA: TBD

TA's email: TBD

TA Office: TBD

TA's office hours:

Credits: 3

Structure:

Two 75-minute lectures per week. For the assignments and the course project substantial lab work using CAD tools will be involved.

Prerequisites:

Students are expected to have working knowledge of logic design, elementary circuits and basic device physics. Background in computer architecture is helpful, but not required.

Topics:

- MOS Transistors
- MOS Inverter Circuits
- Static MOS Gate Circuits
- High-Speed CMOS Logic Design
- Transfer Gate and Dynamic Logic Design
- Semiconductor Memory Design

- Advanced Devices beyond CMOS

Textbook:

CMOS VLSI Design, Weste and Harris, Fourth Edition

Additional Reference:

Analysis and Design of Digital Integrated Circuits - In Deep Submicron Technology, Hodges, Jackson and Saleh, McGraw-Hill, Third Edition, 2004.

J. M. Rabaey, A. Chandrakasan, and B. Nikolic, Digital Integrated Circuits: A Design Perspective. Second Edition, Prentice Hall, 2003.

Grading:

Home assignments	20%
Lab assignments	20%
Project	20%
Midterms	20% (10% each)
Final exam	20%

Late submission: -5%/day, maximum -50%.

Students with Disabilities: Reasonable accommodations are available for students with a documented disability. If you have a disability and may need accommodations to fully participate in this class, please visit the Disability Resource Center (DRC). All accommodations **MUST** be approved through the DRC (Admin Annex Bldg, Room 205). Please stop by or call 509-335-3417 to make an appointment with a disability specialist.

Academic Integrity: The School of Electrical Engineering and Computer Science Academic Integrity Policy will apply to this course. In summary, the policy provides that EECS faculty who observe instances of academic dishonesty, i.e., cheating, will have the full range of options available to them that are outlined in the Student Handbook (including assigning a failing grade for the course). Additionally, faculties are

encouraged to report all instances of academic dishonesty to either the Graduate or Undergraduate Program Coordinators, whichever is appropriate. Students who commit acts of academic dishonesty in an EE or CptS course who have not been certified may be ineligible for certification, while certified undergraduates may be decertified. Ignorance of these consequences or of the definition of academic dishonesty in a particular class does not serve as an excuse. Students who observe acts of academic dishonesty may report their observations to the course instructor or to the Associate Director of the School.