

# Low-Swing Interconnect Interface Circuits

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## 1. ABSTRACT

This paper reviews a number of low-swing on-chip interconnect schemes, and presents a thorough analysis of their effectiveness and limitations. In addition, several new interface circuits, presenting even more energy savings, are proposed. Some of these circuits not only reduce the interconnect swing, but also use very-low supply voltages, so as to obtain quadratic energy savings. The performance of each of the presented circuits is thoroughly examined using simulation on a benchmark interconnect circuit. Energy savings with a factor of seven have been observed for some of the schemes.

## 2. INTRODUCTION

In the deep-submicron era, interconnect wires (and the associated driver and receiver circuits) are responsible for an ever increasing fraction of the energy consumption of an integrated circuit. Most of this increase is due to global wires, such as busses and clock and timing signals. This observation is particularly true for reconfigurable circuits. For instance, it has been observed that more than 90% of the power dissipation of traditional FPGA components (over a wide range of applications) is due to the interconnect [1]. For gate array and cell library based designs, Dake Liu [8] found that the power consumption of wires and clock signals can be up to 40% and 50% of the total on-chip power consumption respectively.

Obviously, techniques that can help to reduce these ratios are very desirable. Short of reducing the average length of the wires and their fanout by using advanced processes or improved architectures, reducing the voltage swing of the signal on the wire is the best bet towards getting better energy efficiency. In this paper, we will analyze the effectiveness of a number of reduced swing interconnect schemes that have been proposed in the literature [2-6]. In addition, a number of novel or modified circuits will be introduced, simulated, and critiqued. To present a fair and realistic base for comparison, a single test circuit will be

used. Overall, it is found that the proposed schemes present a wide range of potential energy reductions, yet that other considerations such as complexity, reliability, and performance play important roles as well.

The paper is organized as follows. In section 3, the test bed that will be used in all simulations is presented. This is followed by a review and comparison of a number of architectures, obtained from the open literature. Several novel or modified low-swing schemes are proposed and analyzed in section 5. Finally, section 6 brings them all together and draws some conclusions.

## 3. TEST ARCHITECTURE AND QUALITY METRICS

Presenting a fair comparison for the various interconnect schemes that are presented in this paper requires a common and fair test-bed. Fig. 1(a) illustrates the schematic of our benchmark interconnect circuit. The driver converts a full-swing input into a reduced-swing interconnect signal, which is converted back to a full-swing output by the receiver. The interconnect line is a metal-3 layer wire with a length of 10 mm, modeled by a  $\pi$ 3 distributed RC model with an extra capacitive load  $C_L$  distributed along the wire (for fanout), as shown in Fig. 1(b). To fairly compare the delays of different schemes, we deliberately add an inverter prior to the driver and an inverter after the receiver with 20 fF capacitive load. Both inverters are sized with  $W_p=6 \mu\text{m}$  and  $W_n=3 \mu\text{m}$ . All circuit comparisons are based on the MOSIS HP CMOS14TB process parameters and spice models. The minimum drawn channel length for this process is set to 0.6  $\mu\text{m}$  with an effective channel length of 0.5  $\mu\text{m}$ .

While energy minimization is the ultimate goal of our study, a range of other metrics have to be considered to make the analysis meaningful.

- Energy — The dynamic energy of the interconnect is given by (EQ 1). When comparing schemes with differ-

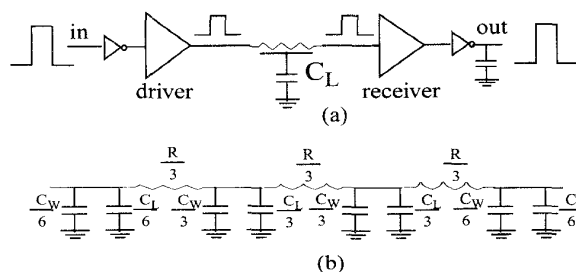


FIGURE 1. (a) Benchmark test architecture; (b) Interconnect model.

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ent types of circuit design such as dynamic design versus static design, differences in data activity should be taken into account.

$$E_{dyn} = (C_W + C_L) \cdot V_{DD}(driver) \cdot V_{swing} \quad (EQ 1)$$

- Area and design complexity.
- Speed.
- Reliability — Three main sources of reliability degradation have to be considered: process variation, voltage supply noise, and inter-line crosstalk. As for process variation, the most important parameters are the threshold voltage variation and mismatch of transistors. For each circuit, we consider the corner cases and perform a Monte Carlo analysis with a 10% VDD fluctuation and 10% threshold voltage variation. For the crosstalk noise due to interline coupling, we only examine the worst-case scenario: a single global line in parallel with two minimum-spaced neighboring wires.

#### 4. REVIEW OF EXISTING LOW-SWING INTERFACE CIRCUITS

In this section, seven low-swing circuit schemes (3 static and 4 dynamic) are reviewed, and the pro's and con's of each approach are enumerated. The important design metrics of the circuits are compared based on simulation results.

##### 4.1 Static Driver With Reduced Supply

The Conventional Level Converter (CLC) shown in Fig. 2 represents the traditional way of converting a low-swing signal back to a full swing one. The driver uses an extra supply with lower voltage to drive the interconnect from 0 to  $V_{DD_L}$ . Although the noise margin is reduced, this circuit is very robust against noise, since the receiver behaves as a differential amplifier, and the internal inverter further attenuates some noise through regeneration. The Symmetric Driver and Level Converter (SDLC), proposed in [2], also falls in the same category. It needs two extra power rails to limit the interconnect swing, and uses special low- $V_T$  devices ( $\sim -0.1V$ ) to compensate for the current-drive loss due to the lower supplies.

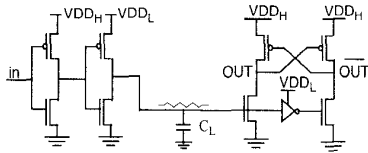


FIGURE 2. Conventional level converter

##### 4.2 Differential Interconnect (DIFF)

Differential signaling has better noise immunity due to its common mode rejection, allowing for a further reduction in the signal swing. Fig. 3 shows a circuit proposed in [9], which produces quadratic energy savings by using a very-low voltage supply. The driver uses NMOS for both pull-up and pull-down. The receiver is an unbalanced current-latch sense amplifier. The receiver adds area overhead, and it consumes energy at every clock-cycle. Therefore, for short interconnect wires with small capacitive load, the receiver-

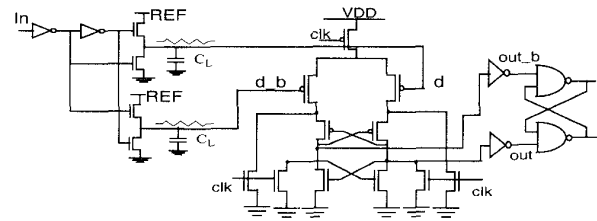


FIGURE 3. Differential low swing interconnect

overhead may become dominant. The operation of the sense amplifier is sensitive to mismatches between devices P1 and P2, but not to the supply noise. In general, one problem with differential schemes is that the number of wires is doubled, which certainly presents a major concern in most designs. Another overhead is the extra clock signal.

##### 4.3 Dynamically-Enabled Drivers

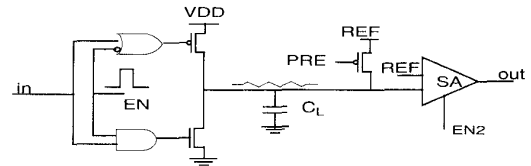


FIGURE 4. Pulse-controlled driver with sense amplifier

In this category, the basic idea is to control the (dis)charging time of the drivers so that a desirable swing on the interconnect is obtained. The Pulsed-Controlled Driver (PCD) showed in Fig. 4 is a typical member of this class. The advantage of this circuit is that the pulse width can be fine-tuned to realize a very-low swing while no extra voltage supply is needed. However, it only works well if the capacitive loads are well-known beforehand. Furthermore, the wire is floating when the driver is disabled, making it susceptible to noise. The *RSD\_VST* scheme, proposed in [5] also dynamically controls the driver, but with an internal control signal. The driver uses an embedded copy of the receiver circuit (called a *Voltage-Sense Translator* or VST), to sense the interconnect swing so as to provide a feedback signal to control the driver. This circuit has a potential problem due to the wire delay: the output of the driver may reach a certain voltage level first and disable the driver, before the input of the receiver is at the right level to switch the receiver. Potential  $V_T$  mismatches between the two VSTs and supply noise can cause a similar problem. Moreover, the floating interconnect (when the driver is disabled) is vulnerable to noise.

##### 4.4 Low Swing Bus

The *Charge Inter-Shared Bus* (CISB) [3] and *Charge-Recycling Bus* (CRB) [4] are two schemes that reduce the interconnect swing by utilizing charge-sharing between multiple data bit-lines of a bus. The CRB scheme uses differential signalling while the CISB is single-ended. Both schemes reduce the interconnect swing by a factor of  $n$  (where  $n$  is the number of bits). The Charging-Recycling Bus approach presents quadratic power savings (by a factor of

$n^2$ ), although the potential savings are offset by the fact that the energy dissipation is constant, independent of the signal activity (the bus is (dis)charged for every cycle). Both of their receivers use complicated current-latch sense amplifiers, and the required timing signals add more complexity. One stringent requirement for these bus schemes to work reliably is that all the wire capacitances must be matched very well, which is certainly non-trivial in real system designs. In both schemes, but especially in *CRB*, noise immunity is compromised by the floating of the interconnect in-between cycles.

#### 4.5 Comparison

Simulated results for each of the presented circuits, accompanied by their key features, are tabulated in Table 1. The *CMOS* scheme in the first row represents the full swing case. In general, the schemes with static drivers have better noise immunity. *PCD* is only feasible for systems with well-characterized interconnects. *CLC* is very robust and can reduce energy by 60% of the original at the expense of an extra lower voltage supply. The *SDLC* scheme can reduce the energy by 70%, with low- $V_t$  devices and two reference voltages. The *CISB* and *CRB* schemes are only suitable for multiple-bit bus units with large capacitive load. Simulation results predict energy savings of up to 3.5 times. Both of them are slow compared to the other schemes due to the charge-sharing mechanism. The *RSD\_VST* scheme can dynamically change the swing depending on the capacitive load and the sensitivity of *VST*, while is susceptible to device mismatch and other noise. The *DIFF* scheme uses a very low voltage supply to achieve quadratic energy savings. However, it is not suitable (in general) for on-chip interconnection because of its dual line structure and the overhead of the sense amplifier.

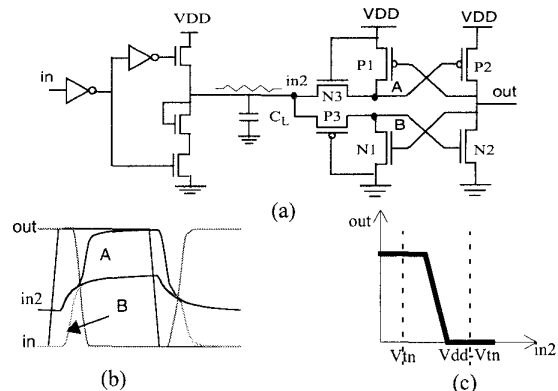
Schemes	Energy (PJ)	Delay (ns)	E•D (PJ•ns)	Swing (V)	Robustness	Complexity
CMOS	11.6	2.1	24.3	2.0	excellent	least
CLC	4.4	3.1	13.6	1.1	very robust	1 REF
SDLC	3.6	2.4	8.6	0.5	reliable	low- $V_t$ devices, 2 REFs
DIFF	2.5	3.0	7.5	0.2	reliable	extra timings, 1 REF, wires doubled
PCD	3.5	2.0	7.0	0.5	only for known $C_L$	extra controls
RSD_VST	3.7	2.0	7.4	0.6	not reliable	1 REF, big driver
CISB	3.5	4.4	15.4	0.25	small margin, only for multi-bit bus	extra timings, sense amplifiers
CRB	3.1	3.5	10.9	0.25	not reliable, only for multi-bit bus	extra timings, wires doubled

**Table 1: Performance Comparison ( $V_{dd}=2V$ ,  $C_L=1PF$ )**

### 5. PROPOSED INTERFACE CIRCUITS

We now present several modified or novel low-swing interconnect interface circuits to address some problems of the earlier schemes. For robustness sake, we only selected static drivers and avoided floating interconnect. The first two schemes use a single supply voltage for the drivers, while the rest need extra supplies. These can be realized on-chip with power-efficiencies around 90% [7]. The last two schemes need additional timing signals.

#### 5.1 Symmetric Source-Follower Driver with Level Converter (SSDLC)



**FIGURE 5. (a) Symmetric source-follower driver with level converter; (b) Simulated waveforms; (c) Voltage transform curve**

The *SSDLC* scheme is shown in Fig. 5(a). The driver limits the interconnect swing from  $V_{tn}$  to  $V_{dd}-V_{tn}$ , shown as node *in2* in Fig. 5(b). The basic idea of the symmetric level converter is similar to the one in *SDLC* circuit, except that the gates of those two pass transistors *N3* and *P3* are biased at  $V_{dd}$  and Ground respectively. Moreover, no special low- $V_t$  devices are needed in this circuit. Assume that node *in2* goes from low to high;  $V_{tn}$  to  $V_{dd}-V_{tn}$ . Initially, node *A* sits at  $V_{tn}$  and node *B* sits at Ground. During the transition period, with both *N3* and *P3* conducting, *A* and *B* rise to  $V_{dd}-V_{tn}$  as shown in Fig. 5(b). Consequently, *N2* is turned on, and *out* goes to low. The feedback transistor *P1* pulls *A* further up to  $V_{dd}$  to cut off *P2* completely. *in2* and *B* stay at  $V_{dd}-V_{tn}$ . Note that there is no current path from  $V_{dd}$  to Ground through *N3* although the gate-source voltage of *N3* is nearly  $V_{tn}$ . Since the circuit is symmetric, the same explanation can be applied to the case of high to low transition. If ignoring feedback transistors *P1* and *N1*, the DC voltage transform curve (VTC) of the level converter is virtually a truncated version of that of the *P2-N2* pair, as shown in Fig. 5(c). The predicted energy-savings ratio of the interconnect is defined in (EQ2):

$$\frac{E_{new}}{E_{full}} = \frac{V_{dd} - V_{tn} - V_{tn}}{V_{dd}} \quad (\text{EQ 2})$$

To obtain reasonable noise margins,  $V_{dd}$  is set at 2.4V in our simulation, which gives an interconnect swing of 0.7V. The sensing delay of the receiver is as small as two inverter delays. This circuit is very robust with respect to the supply noise and device variation. Moreover, no extra internal supplies are needed.

#### 5.2 Static Driver with VST (SDVST)

Fig. 6 shows the circuit diagram of the *SDVST* scheme. The driver drives the interconnect with a swing from  $REF_L$  to  $V_{dd}-V_{tn}$ , where the threshold voltage is subject to the body effect. The internal voltage supply  $REF_L$  is set below  $V_{tn}$  of

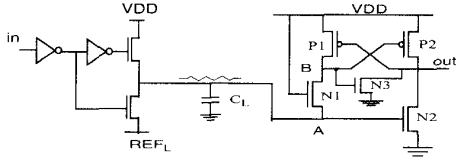


FIGURE 6. Static driver with VST

N2. The receiver is a modification of the VST, and is actually an asymmetric version of the level-converter in the *SSDLC* scheme. Their operations are same in the case of low-to-high transition. For the case of high-to-low transition, after *A* and *B* are discharged to a voltage level below  $V_t$  of transistor N2, N2 is turned off, and P2 pulls *out* up to  $V_{dd}$ . Transistors P2 and N2 are sized wide enough to have a large transconductance in order to quickly sense the small  $V_{gs}$  applied on them. The feedback transistor N3 is to provide more current drive to discharge the output. The following energy-savings ratio is obtained:

$$\frac{E_{new}}{E_{full}} = \frac{V_{dd} - V_{tn} - REF_L}{V_{dd}} \quad (\text{EQ 3})$$

Compared to *RSD\_VST* scheme, *SDVST* is more robust because its driver is static.

### 5.3 Level Converter with Low- $V_t$ Device (LCLVD)

Fig. 7 shows the schematic diagram of the *LCLVD* scheme. In this scheme, the receiver is the same as the one in *CCL* scheme discussed in section 4.1, except that it uses low- $V_t$  devices for N1, N2 and the internal inverter. Because *inb* is slower than *in2*, the two branches are designed asymmetrically to balance the switching delays in different directions. N2 is sized larger than N1, and P1 larger than P2. The ratio of energy savings is given by (EQ 4):

$$\frac{E_{new}}{E_{full}} = \left( \frac{REF}{V_{dd}} \right)^2 \quad (\text{EQ 4})$$

In our simulation, REF is set at 0.7 V. and  $V_{tn}$  and  $|V_{tp}|$  of the low- $V_t$  devices are set at 0.3 V. Simulation at the process corners proves that this circuit is very reliable against supply noise and process variation. The receiver behaves like a differential sense amplifier by regenerating a complementary input signal internally.

### 5.4 Capacitive-Coupled Level Converter (CCLC)

The *Capacitive-Coupled Level Converter* (CCLC) scheme, shown in Fig. 8(a), uses a coupling capacitor to boost the

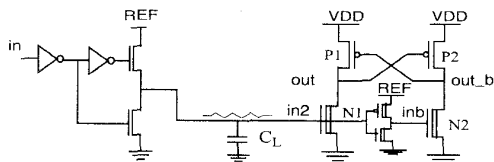
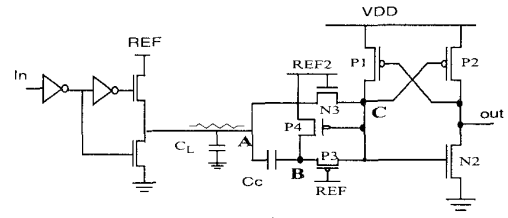
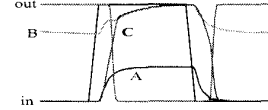


FIGURE 7. Level converter with low- $V_t$  devices



(a)



(b)

FIGURE 8. a) Capacitive-coupled level converter; (b) Simulated waveforms

low-swing signal so that the NMOS transistor of the receiver can be turned on.  $REF2$  is set to be less than  $(REF + V_{tn})$ . When *A* switches from high to low, pass transistor N3 is turned on, thus *C* is pulled down to Ground. *out* is pulled up to  $V_{dd}$  with transistor N2 turned off and P2 on. With pass transistor P4 conducting, *B* is set to  $REF2$ . Since the gate-source voltage across P3 is less than its threshold voltage, P3 is not conducting, and therefore no static current path exists. When *A* goes from low to high, the coupling capacitor  $C_c$  couples a voltage jump onto *B*. Meanwhile, pass transistor N3 is turned off. *C* rises up by charge sharing with *B* through P3, as shown in Fig. 8(b). With *out* being pulled low by N2, P1 pulls *C* and *B* further up to  $V_{dd}$ .

The ratio of energy savings is given by (EQ 4). In the simulations,  $REF$  and  $REF2$  are set as 0.7 V and 1.2 V, respectively. The coupling capacitor  $C_c$  is set as 0.2 pF to provide enough coupling effect in the presence of charge sharing between  $C_c$  and parasitic capacitances. However, the operation of this circuit is not very sensitive to variations in  $C_c$ . The receiver has a relatively small noise margin due to its susceptibility to the device variation.

### 5.5 Pseudo-Differential Interconnect (PDIFF)

Fig. 9 shows the circuit diagram of the *PDIFF* scheme [9]. The gates of P1 and P3 are connected to *d*, while the gates of P4 and P2 are biased at Ground and  $REF$  respectively. Initially, *clk* discharges *n1*, *n2*, *A*, and *B* to Ground. After *d* is driven to the desired level, the receiver is enabled by a negative pulse of *clk*. If *d* is low, the current drive of P3 is same as that of P4, while the current drive of P1 is larger than that of P2. As a result, *B* is pulled high and *A* is pulled low. An opposite transition is triggered when *d* is high. The obvious advantage over the *DIFF* scheme is that the number of wires is cut to half. However, the swing of the interconnect has to be increased to compensate for the loss in immunity to common mode noise. The energy-savings ratio is given in EQ. (4).  $REF$  is set at 0.6 V in the simulations. The receiver is very robust against the supply

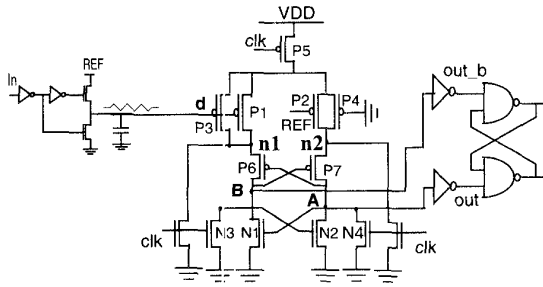


FIGURE 9. Pseudo-differential interconnect;

noise and device variation, because of its symmetric nature with double input transistor pairs.

### 5.6 Level-Converting Register (LCR)

Fig. 10(a) shows the circuit diagram of the *LCR* scheme. The receiver consists of a cross-coupled inverter pair, with one precharge transistor P3 and one pass-transistor N3, whose gates are controlled by two timing signals PRE and EVAL, respectively. Typical waveforms are shown in Fig. 10(b). Initially, a negative pulse PRE is applied to P3 to precharge node *A* to *Vdd* and discharge node *out* to Ground. After the input signal reaches stable at node *d*, a positive pulse EVAL is applied to N3. The high end of the voltage swing of EVAL is set to be less than  $REF + V_{tn}(N3)$ . If *d* is high, N3 stays off, and the state of the inverter pair remains the same. In the case of *d* being low, N3 starts conducting, and pulls *A* low, thus the state of the inverter pair is flipped over. After EVAL switches back to low, N3 is cut off, and the inverter pair keeps the data as a static register. The receiver is level sensitive, so that when EVAL is active, the inverter pair will switch its state by a high to low glitch on the interconnect, and can not switch back by bringing the

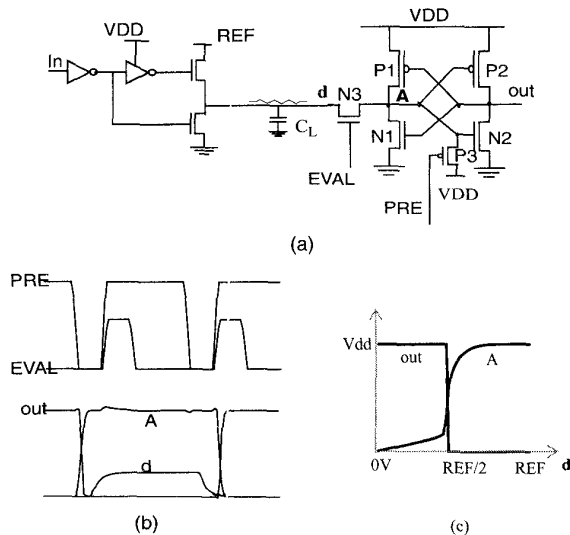


FIGURE 10. (a) Level-Converting Register; (b) simulated waveforms; (c) voltage transform curve

input back to high. Therefore, the EVAL pulse has to be as narrow as possible to avoid such an error. Fig. 10(c) illustrates the DC voltage transform curves of the receiver, with the gate voltages of the feedback transistors P1 and N1 set to Ground.

A major advantage of this simple receiver is that it combines the functions of a level converter and a register. It has little area overhead, although the extra timing signals increase its complexity. The matching of the current drive capabilities of the P1-N3 pair is critical to receiver's noise margin, which is susceptible to supply noise and  $V_t$  variations. However, as long as EVAL is applied after the input of the receiver reaches stability, the receiver works well. This circuit can be used for both synchronous and asynchronous signalling, given the timing signals PRE and EVAL are generated correctly.

### 5.7 Simulation Results and Comparison

To compare the six proposed schemes, two sets of simulations were performed. For all the simulations, we used the test structure of Fig. 1(a). In the first set of simulations,  $V_{dd}$  is set at 2V for all the schemes except for *SSDLC* ( $V_{dd}=2.4V$ ), and the capacitive load on the interconnect is swept from 0 to 5 pF with the transistor sizes kept constant. The simulation results are illustrated in Fig. 11. From the *Delay* vs.  $C_L$  plots, it can be seen that the proposed schemes have similar performance and that their delays increase linearly with  $C_L$ . From the *energy* vs.  $C_L$  plots, it can be observed that the energy values increase linearly, but with different slopes. *LCR* scheme consumes the least, reducing the energy with a factor of 7. *SSDLC* and *SDVST* can cut the energy by half, while *LCLVD*, *CCLC*, and *PDIFF* provide a factor of up to 5. The energy-delay products display a similar ranking. In the second set of simulations,  $C_L$  is set to 1 pF, while the supply voltage is swept from 1.5 V to 3.3 V. For the full-swing schemes (*CMOS*, *SSDLC* and *SDVST*), the transistor sizes are kept unchanged. For others, the transistors have to be resized to optimize their operation for different supply voltages. The

Schemes	Energy (pJ)	Delay (ns)	E·D (pJ·ns)	Swing (V)	Robustness	Complexity
CMOS	11.6	2.11	24.5	2.0	excellent	least
SSDLC ( $V_{dd}=2.4V$ )	6.89	2.73	18.8	0.7	works for variable VDDs	some area overhead
SDVST	4.79	2.38	11.4	0.7	works for variable VDDs	1 REF
LCLVD	2.43	2.49	6.05	0.7	good noise margin	Low- $V_t$ devices, 1 REF
CCLC	2.36	2.47	5.84	0.7	small noise margin	coupling capacitor, 2 REFs
PDIFF	2.69	2.86	7.7	0.6	reasonable noise margin	big receiver, timings, 1 REF
LCR	1.78	2.43	4.32	0.6	reasonable noise margin	timings, 2 REFs

Table 2: Performance Comparison ( $V_{dd}=2V$ ,  $C_L=1PF$ )

results are shown in Fig. 12. *CCLC* only works well for  $V_{dd}$ 's between 1.8 V and 2.5 V, and *SSDLC* only works for  $V_{dd}$  higher than 2.4 V. The ranking of the energy and

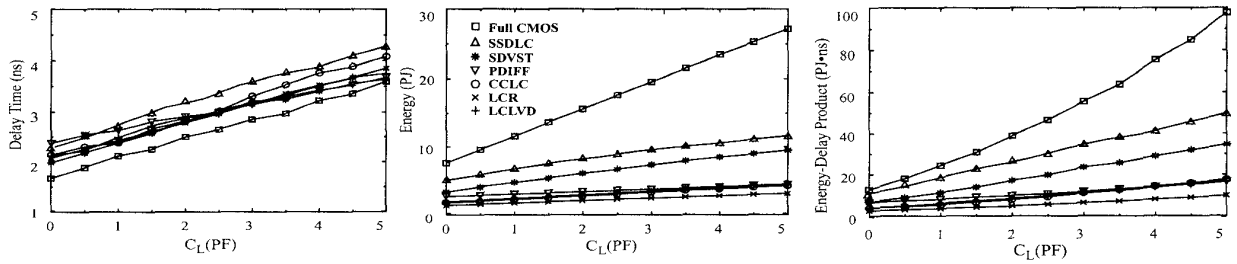


FIGURE 11. Delay, Energy, Energy-Delay product vs. Capacitive load of interconnect, at  $V_{dd}=2V$

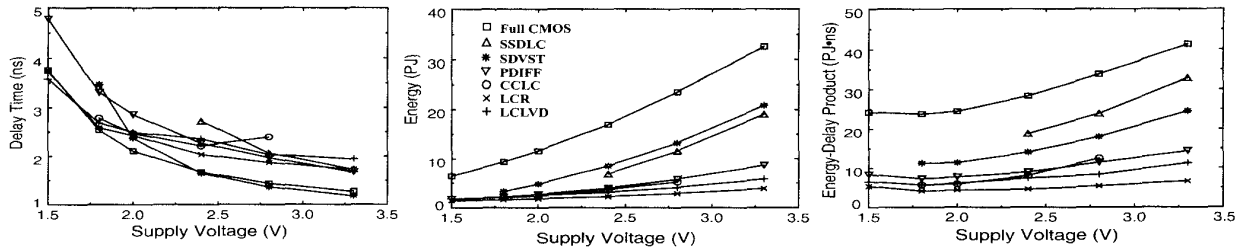


FIGURE 12. Delay, Energy, Energy-Delay product vs. Supply voltage, at  $C_L=1\text{ PF}$

energy-delay product is the same as in the first set of simulations. Note that the *LCF*, *PDIFF*, and *LCLVD* schemes display almost-flat energy and energy-delay product curves for the whole range. The performances of the different schemes are tabulated in Table 2 for the parameter settings of  $V_{dd} = 2\text{ V}$ ,  $C_L = 1\text{ pF}$  (except for *SSDLC* with  $V_{dd}=2.4\text{ V}$ ).

## 6. CONCLUSION

Existing low-swing interconnect interface-circuit schemes show a wide variety of problems in both efficiency, performance, and robustness. We have introduced a number of novel or modified circuits to address some of these problems, or to get even higher energy savings. The *SSDLC* and *SDVST* schemes can reduce the energy consumption up to 60% without much overhead while possessing good robustness. The *LCLVD* scheme can produce energy savings by a factor of 5 if low- $V_t$  devices are available while also having a good noise margin. *CCLC* also gets a 5 times energy reduction without requiring extra timing signals, but comes with a large area overhead and a small noise margin. Finally, the *PDIFF* and *LCR* schemes show great promise for both synchronous and asynchronous system design, potentially reducing the energy by a factor of seven! In summary, low-swing interconnect is an effective tool for minimizing energy dissipation, but requires a judicious optimization with respect to robustness, design complexity, and energy reduction.

## 7. ACKNOWLEDGEMENTS

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