

Determining Mechanical Stress Testing Parameters for FHE Designs with Low Computational Overhead

Ganapati Bhat, Hang Gao, Sumit K. Mandal, Umit Y. Ogras, and Sule Ozev
School of Electrical, Computer, and Energy Engineering
Arizona State University
 Tempe, AZ, USA
 {gmbhat, hgao44, skmandal, umit, sule.ozev}@asu.edu

Index Terms—Flexible hybrid electronics, test, COMSOL Multiphysics, stress, integer linear programming

I. INTRODUCTION

Flexible hybrid electronics (FHE) is an emerging technology which combines the form-factor advantages of flexible electronics with performance similar to traditional CMOS technologies [1]. FHE achieves this by integrating rigid ICs, such as in a micro-controller, on a flexible substrate. Due to this integration, FHE devices can achieve high performance while maintaining their ability to bend and stretch. FHE devices have been used in a number of interesting applications such as activity and health monitoring [2].

FHE devices undergo multiple types of bending and twisting conditions which can affect the performance of the device. For instance, the bending of a flexible photovoltaic cell reduces the maximum power point by as much as 56% [3]. Similarly, bending can damage the solder joints. Therefore, the effects of bending have to be taken into account during the design process of the device [4].

FHE devices also have additional test requirements compared to the traditional rigid systems. Rigid boards are typically tested on a flat surface using interfaces such as Joint Test Action Group ports [5]. As a result, the device-under-test does not experience any mechanical stress during testing. In contrast, FHE devices can experience significant stress during their routine operations, which need to be duplicated in the test environment. Variations in electrical characteristics need to be characterized under bending. Moreover, since mechanical stress can lead to fractures in the solder joints and traces [6], the functionality should be tested under various bending scenarios.

Recent research considered methodologies to perform mechanical stress testing of FHE devices [7, 8, 9]. These setups typically fix one side of the board and apply force on the other side. Depending on the size of the board, the possible positions for the fixed point and the force can take different values. If the board has n positions along the edge, a total of $O(n^2)$ combinations are possible for choosing the fixed point and the point where force is applied. Figure 1 shows an example of a simple board with 12 solder joints and three

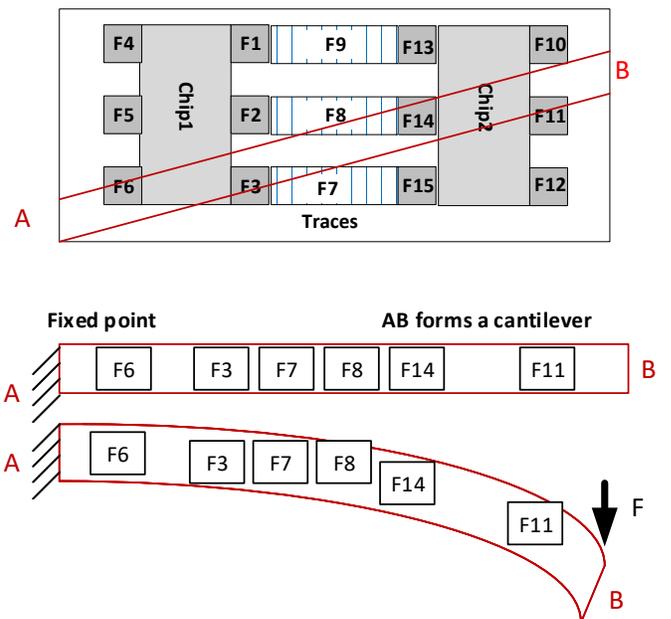


Fig. 1. An illustrative example of an FHE board with rigid components, solder joints, and traces generating potential parametric and catastrophic faults along the chosen mechanical stress pattern AB.

traces, each of which can be a potential fault. In this figure, force F is applied at point B while fixing point A, thus forming a cantilever along the line joining points A and B. Force F creates varying degrees of stress on fault locations. The stress experienced by faults changes when the positions of A and B are changed. Therefore, a mechanical stress testing device needs to re-position the device for each possible combination of A and B, leading to a high test cost and low throughput. Therefore, there is a strong need to develop methodologies that can minimize the time required to perform stress testing of the device.

The goal of this paper is to optimize the mechanical stress patterns required to adequately test all the potential fault locations on an FHE device. We reduce the number of cantilevers that need to be tested mechanically by utilizing two key insights. First, we observe that each fault resides in the path of multiple stress patterns. Therefore, we eliminate the patterns that stress redundant faults. Second, faults need to be

stressed to a minimal level to emulate real-world conditions. The minimum stress requirement can be obtained using the radius of curvature specifications dictated by the application. This minimal level of stress is not exerted by all cantilever beams, hence, they can be eliminated from the test process. Using these two insights, we find the minimum number of stress patterns that cover all the fault locations. We validate our approach on an in-house FHE prototype. We use the COMSOL multiphysics environment to obtain stress conditions for each fault location. Then, we develop a high-level model to estimate the stress for unsimulated cantilever beams such that the testing time can be further reduced. Finally, we formulate a heuristic solution to optimize the stress patterns with low computational overhead.

II. RELATED WORK

The development of FHE devices comes with the additional challenge of testing them under various bending and twisting conditions. However, testing FHE devices under multiple bending and twisting conditions is challenging. This is typically achieved by applying mechanical stress on the device and analyzing the effect of the stress. Recent studies have used three types of mechanical stress, convex and concave radius of curvature, and torsional stress [10] to test FHE devices. Wen et al. [7] present a mechanical stress unit to characterize the electrical performance of the device under mechanical stress. Similarly, a device to bend an FHE device along its length or width is presented in [8]. Experiments using the device show that significant changes in electrical characteristics occur under bending stress. Lall et al. [6] emulate different application-specific scenarios, such as bending of the arm. Using the mechanism, the authors perform electrical tests before, during, and after bending the FHE device. These experiments show that FHE devices exhibit significant variations in solder characteristics during bending. While these approaches are useful to evaluate FHE devices, they rely only on mechanical stress patterns to test the devices. However, application of all possible test patterns is time-consuming and not practical. Therefore, our prior work first performs COMSOL simulations and then determines an optimal set of mechanical stress patterns that sufficiently cover possible bending scenarios [9]. This paper further improves simulation time by building a neural network model to estimate the stress experienced by the faults. Moreover, we propose an efficient heuristic to solve the problem of optimizing the stress patterns. These techniques lead to significant savings in terms of test time and improve throughput.

III. MECHANICAL STRESS TEST GENERATION FRAMEWORK

A. Methodology

Testing of FHE devices using mechanical stress and bending is crucial to ensure that the devices do not fail during their operation. We model the stress experienced by FHE devices by fixing a point along an edge of the device and applying a force at another point on the device. The fixed point and the force form a beam that is bent due to the force. This emulates

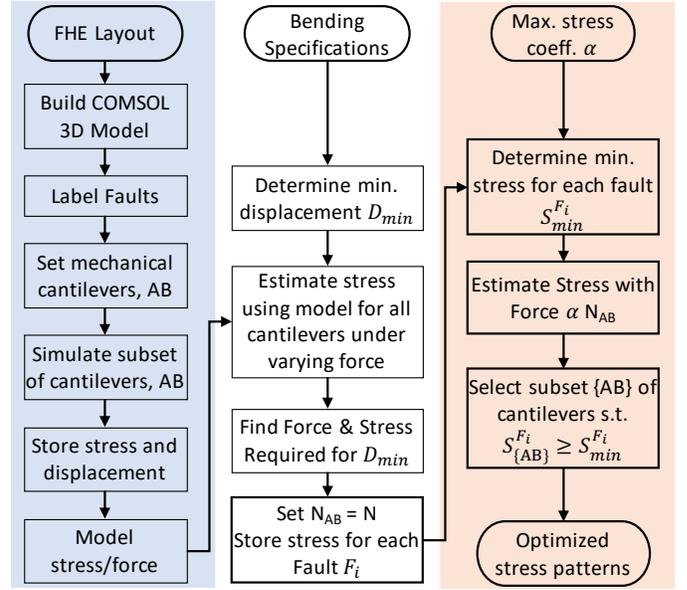


Fig. 2. Flow of the proposed mechanical stress optimization methodology

the bending and twisting experienced by FHE devices. This test can be performed by applying mechanical stress in a laboratory. However, measuring each possible scenario is time-consuming and impractical. Hence, we propose a technique using COMSOL multiphysics simulator [11] to evaluate the stress at various locations on the device.

Figure 2 shows the flow of the proposed optimization approach. We take the FHE device layout, bending specifications, and the maximum stress coefficient α as the inputs. The maximum stress coefficient allows us to *overstress* a given fault. Using the FHE layout, we build the 3D model in COMSOL. Next, we label all faults in the layout. After identifying the faults, we identify the cantilever beams AB on which the force is applied. In order to obtain the cantilever beams, we need to fix the width of each cantilever beam. We find this width by determining the length over which the stress is similar in the vertical direction with respect to the line formed by AB. Simulating each possible cantilevers can lead to high simulation time. For instance, we have a total of 192 cantilevers on our experimental board. Therefore, we first simulate a subset of cantilevers. After each simulation, we store the stress experienced by each fault and the displacement of the board. Then, we use this data to train a neural network that can estimate the stress per unit force for a given fault. This model is then used to obtain stress for other cantilevers.

Next, we obtain the stress experienced by the faults under the remaining cantilevers (not used in training) using the trained neural network. Using this data, we determine the force N required to achieve the minimum displacement as per the bending specification. This force is then stored along with the stress at each of the faults. We analyze the stress at each fault F_i to find the minimum required stress $S_{min}^{F_i}$ as the maximum stress experienced by the fault across all the cantilevers. Since our goal is to minimize the number of cantilevers for mechanical testing, we also increase the

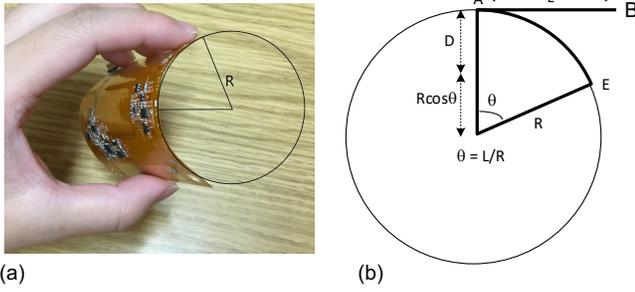


Fig. 3. Determining required displacement, D , from the given bending specifications as radius of curvature, R , and the cantilever length, L .

minimum force N by a factor of α and estimate the stress at the increased force. Finally, we select a subset of cantilevers $\{AB\}$ such that each fault experiences the minimum required stress. This reduced set of patterns can then be mechanically tested before the device is released for manufacturing.

B. Radius of Curvature and Displacement

The flexibility requirement of an FHE device depends on the intended application. For example, a device to be worn on the wrist has different bending requirements compared to a device intended for shoulders. Therefore, we use the application requirements to determine the radius of curvature (ROC) R of the FHE device. This process is illustrated in Figure 3(a).

To perform simulations, we fix one end of the cantilever and apply force at the other end. This leads to a displacement at the location where the force is applied. The displacement experienced by the FHE device must match the ROC requirements of the application, as illustrated in Figure 3(b). Figure 3 shows a cantilever with endpoints A and B, respectively. When the force is applied at point B while keeping A fixed, the cantilever bends to the point E shown on the circle. Here, D represents the displacement of cantilever's moving end, and R represents the radius of curvature. Furthermore, the arc AE and the cantilever have the same length, leading to a central angle θ . Using the angle, we can determine the displacement D as:

$$D = R\left(1 - \cos \frac{L}{R}\right) \quad (1)$$

where L is the length of the cantilever and R is the radius of curvature. The displacement obtained using this equation is provided as an input to the optimization framework in Figure 2.

C. Modeling of Stress in Beams

The proposed methodology requires simulating multiple cantilevers while applying varying levels of force. These simulations can result in significant runtime overhead if the designer simulates each condition. Simple analytical models [12] for stress in a cantilever are also not suitable since cantilever beams on FHE devices may contain many rigid ICs, which change the stress at different points on the beam. Therefore, we propose a high-level modeling framework using neural

networks to estimate the stress at a fault without performing the detailed simulations.

We start the modeling by first evaluating the different types of cantilevers, such as horizontal, vertical, and diagonal. Then, for each type of cantilever, we simulate a subset of all available cantilevers while sweeping the applied force. We record the stress at each fault location for all the simulated cantilevers. A portion of this stress data forms the training set for our machine learning model to estimate the stress for unsimulated beams.

After obtaining the simulated stress patterns for the subset of beams, we incorporate a hierarchical ML-based technique to construct a model to estimate stress. In the first level, the ML model categorizes the given fault location into a cluster. In the second level, the model estimates the stress for the corresponding cluster. We use a neural network to capture the non-linear behavior in the stress observed by different fault locations. The non-linearity occurs due to the presence of rigid ICs on the substrate. Specifically, the rigid ICs provide a shield to all the fault locations that are present beyond the IC. Thus, these fault locations experience lower stress than what they would have experienced if the rigid IC was not present.

Features and parameters of the neural network: The feature set includes the x and y coordinates of the fixed pivot on the IC, the location of the force on a given cantilever, and coordinates of the fault. Coordinates of the middle-point and corners of the IC nearest to the fault are included in the features, since the position of the nearest IC affects the stress experienced by the fault. We also include the slope between the fault location and the location of the force as a feature. Distances between the location of force and fixed point; force and fault; fixed point and fault are also taken as features. All these features are normalized to eliminate any bias in the dataset. These features enable the neural network to adjust the stress estimation when multiple ICs are present between the fault of interest and the force. Using these features and the stress experienced as the label, we train a neural network which categorizes a fault location. Then we train neural networks which estimate stress for each category. We use neural networks with two hidden layers for both classification and estimation of stress. We use categorical accuracy for classification and the mean squared error for estimation as the loss function in the neural networks.

D. Optimization Algorithm

After obtaining the stress experienced by each fault with the required displacement, we move on to the optimization stage of the framework. To this end, we first determine the maximum stress experienced by each fault over all the cantilevers and set it as the minimum stress requirement $S_{min}^{F_i}$. We consider the maximum stress since our goal is to meet the maximum radius of curvature requirement. We can perform the optimization with this stress requirement. However, it may lead to the selection of all cantilevers thus not providing any gains in test time. Therefore, we use the stress multiplier α to stress the faults beyond their minimum requirement. Using the parameter α we increase the force in each cantilever and record the stress under the new force. This ensures that fewer cantilevers are selected for the stress requirement.

Next, we formulate an integer linear programming problem for the optimal selection of cantilevers. To this end, we first define a $N \times M$ coverage matrix A . Here, N is the number of faults, and M is the number cantilevers. If cantilever j stresses a given fault F_i to the minimum required stress $S_{min}^{F_i}$, we set the corresponding entry of the matrix A to 1. Otherwise, we set it to 0. We also define a $N \times 1$ vector b , $M \times 1$ vector c with all entries equal to 1. Finally, we define the optimization variable x as a $M \times 1$ vector. With this setup, the goal of the optimization is to select the minimum number of cantilevers such that the constraints are met. We can express this problem as follows:

$$\begin{aligned} \min \quad & c^T x \\ \text{subject to} \quad & Ax \geq b \\ & x_i \in \{0, 1\} \end{aligned} \quad (2)$$

where the first constraint ensures that the selected cantilevers meet the stress requirement and the second constraint ensures that the values of x are either 0 or 1.

Problem Solution: We solve the optimization problem in Equation 2 using an off-the-shelf ILP solver. However, solving an ILP problem exactly with a large number of cantilevers may incur significant computational overhead for complex FHE boards. Therefore, we propose a heuristic to solve the problem of optimal selection of cantilevers. In this heuristic, we use the matrix A as input. Using this, we sort the cantilevers with decreasing coverage. Then, we visit cantilevers starting with maximum coverage. We select a cantilever (into the optimal set) if it includes at least one fault which has not been covered by the cantilevers visited so far. This process is repeated until either all faults are covered or all cantilevers are exhausted. At the end of execution, we obtain an optimal set of cantilevers which covers maximum possible faults with stress more than the threshold. In Section IV-C, the result obtained from the exact ILP and the proposed heuristic are compared.

IV. EXPERIMENTAL EVALUATION

A. Experimental Setup

The proposed approach is evaluated on the FHE prototype shown in Figure 4. The 3 cm \times 6 cm board includes 12 rigid ICs and the interconnects between them. To obtain the stress under various bending conditions, we construct a 3D layout of the prototype in COMSOL. Then, we simulate the layout by defining cantilever beams on the prototype. For each cantilever beam simulation, we record the stress observed by the faults present on the board. This data is then used for the modeling and optimization of stress patterns required for full coverage of the board.

Cantilevers and Faults: We divide the board into grids to construct the cantilevers for simulation. The width of the grid provides a trade-off between the granularity of the simulation and the simulation time. A higher width for each grid provides lower simulation time at the expense of a loss in detail of the simulation. In this work, we form the grid by first obtaining the minimum spacing required to maintain uniform stress along the width of the cantilever. Specifically, we set the width of each cantilever to 1.5 cm. After determining the cantilevers,

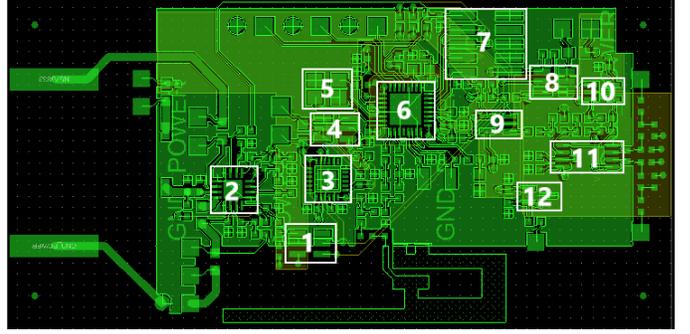


Fig. 4. Prototype FHE Layout where the marked numbers are the rigid chip locations

we define potential fault locations. We choose all the solder-joints as potential fault locations. Additionally, all the traces are chosen as potential faults. Using this approach, we evaluate the stress at a total of 192 potential faults on the chip.

B. Validation of Stress Modeling

To evaluate the accuracy of the model, we train the model with 60% of the data collected and we test with the rest of the data. As described in Section III-C, we first divide the training dataset into five clusters depending on the magnitude of the stress. Then, we train a policy with input as the features of the fault locations and the output as the cluster. This policy classifies a given fault on the substrate into a cluster. Figure 5 shows the accuracy of this policy on the training data for different clusters. On an average, the constructed policy has 97% accuracy to classify a fault into a correct cluster. Furthermore, we train a policy for an individual cluster to estimate the stress per unit force for a given fault. To this end, we first classify the cluster for the fault and then apply the policy for the corresponding cluster to estimate the stress per unit force. The input of the policy are the features of the fault as described in Section III-C. Figure 6 shows the histogram of absolute error between measured and estimated stress per unit force. We observe that 87% of total data points have an absolute error of 0.1 or less where the magnitude of stress varies from very low value to 373.

C. Optimized Cantilever Selection

After performing an initial analysis of the FHE prototype, we determine that a total of 27 cantilevers stress the fault



Fig. 5. Classification accuracy for different clusters.

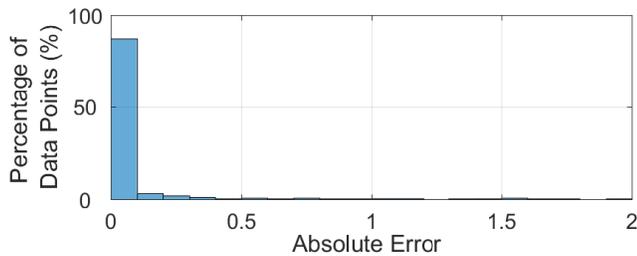


Fig. 6. Histogram of absolute error between stress data obtained from simulation and proposed model.

locations. Using our neural network models, we first obtain the stress experienced by the faults under all the cantilever beams when the radius of curvature requirement of the application is met. We also use the stress multiplier α to obtain the stress under an increased force. Using these stress values, we obtain the coverage matrix A . Then, we use our ILP formulation to select the subset of cantilevers that provide the necessary stress. We obtain the results using an exact ILP solver and our heuristic.

Table I summarizes the results on the experimental device. When α is 1, we only apply the minimum required force based on the ROC specifications, severely limiting the number of cantilevers that can provide this level of stress. 19 out of 27 cantilevers are selected under this condition, resulting in roughly 30% reduction in the number of mechanical stress patterns. Increasing α enables a higher reduction in the number of mechanical stress patterns. Table I also shows the performance of the proposed heuristic which replaces the requirement to solve ILP. Except for $\alpha = 50$, the solution of the proposed heuristic is same as the exact solution. Moreover, the proposed heuristic results in $29\times-50\times$ improvement in the time required to obtain a solution.

TABLE I
NUMBER OF SELECTED MECHANICAL STRESS PATTERNS AND
NORMALIZED EXECUTION TIME WITH DIFFERENT STRESS MULTIPLIERS

Value of α	1	2	5	10	50	100
Exact ILP (no. beams)	19	18	14	13	10	10
Proposed Heuristic (no. beams)	19	18	14	13	11	10
Norm. Exe. Time (ILP/Heuristics)	29	24	50	32	41	50

V. CONCLUSIONS

Flexible Hybrid Electronic devices have found tremendous usage in different domains including medical, and mechanical engineering. Testing these devices is challenging due to the presence of multiple stress patterns. This paper presented a methodology to enable selection of an optimum set of mechanical stress patterns to cover all potential fault locations and exert the required mechanical stress as dictated by the application. Moreover, a modeling technique to estimate stress at various faults is proposed. This modeling technique helps in lowering the simulating time by providing near-accurate estimates of the stress. We validated the proposed approach the stress data using COMSOL on an FHE prototype.

Acknowledgment: This work was supported in part by NSF Grant SHF-1617562, NSF CAREER Award CNS-1651624,

Semiconductor Research Corporation under task ID 2712.003, and DARPA Young Faculty Award (YFA) Grant D14AP00068.

REFERENCES

- [1] U. Gupta, J. Park, H. Joshi, and U. Y. Ogras, "Flexibility-Aware System-on-Polymer (SoP): Concept to Prototype," *IEEE Trans. Multi-Scale Comput. Syst.*, vol. 3, no. 1, pp. 36–49, 2017.
- [2] G. Bhat, R. Deb, V. V. Chaurasia, H. Shill, and U. Y. Ogras, "Online Human Activity Recognition using Low-Power Wearable Devices," in *Proc. Int. Conf. on Comput.-Aided Design*, 2018, pp. 72:1–72:8.
- [3] J. Park *et al.*, "Flexible PV-cell Modeling for Energy Harvesting in Wearable IoT Applications," *ACM Trans. Embedd. Comput. Syst. (TECS)*, vol. 16, no. 5s, p. 156, 2017.
- [4] G. Bhat *et al.*, "Multi-Objective Design Optimization for Flexible Hybrid Electronics," in *Proc. Int. Conf. on Comput.-Aided Des. (ICCAD)*, 2016, pp. 1–8.
- [5] C. W. Yau and N. Jarwala, "A Unified Theory for Designing Optimal Test Generation and Diagnosis Algorithms for Board Interconnects," in *Proc. Int. Test Conf.*, 1989, pp. 71–77.
- [6] P. Lall, J. Narangaparambil, A. Abrol, B. Leever, and J. Marsh, "Development of Test Protocols for the Flexible Substrates in Wearable Applications," in *Proc. IEEE Intersociety Conf. on Thermal and Thermomechanical Phenomena in Electron. Syst.*, 2018, pp. 1120–1127.
- [7] B.-J. Wen and T.-S. Liu, "Bending-Characteristic Measurement of Flexible Electronics by Using Fast Optimal Sliding Mode Control Method," in *Procc of SICE Annual Conference*, 2010, pp. 1872–1874.
- [8] S. Grego, J. Lewis, E. Vick, and D. Temple, "Development and Evaluation of Bend-Testing Techniques for Flexible-Display Applications," *J. of the Society for Information Display*, vol. 13, no. 7, pp. 575–581, 2005.
- [9] H. Gao, G. Bhat, U. Y. Ogras, and S. Ozev, "Optimized Stress Testing for Flexible Hybrid Electronics Designs," in *2019 IEEE 37th VLSI Test Symposium (VTS)*, 2019, pp. 1–6.
- [10] R. L. Chaney, D. R. Hackler, D. G. Wilson, and B. N. Meek, "Physically Flexible High Performance Single Crystal CMOS Integrated with Printed Electronics," in *Proc. IEEE Work. On Microelectronics And Electron Devices (WMED)*, 2014, pp. 1–4.
- [11] R. W. Pryor, *Multiphysics Modeling using COMSOL®: a First Principles Approach*. Jones & Bartlett Publishers, 2009.
- [12] J. Sheats, "Truly Wearable Electronics," in *Proc. of FlexTech Alliance Workshop: Flexible Hybrid Electronics Challenges and Solutions*, July 2014.

Ganapati Bhat received his B.Tech degree in Electronics and Communication from Indian Institute of Technology (ISM), Dhanbad, India in 2012. He is currently a Ph.D. student in Computer Engineering at the school of Electrical, Computer and Energy engineering, Arizona State University. He is a student member of the IEEE and ACM.

Hang Gao received his Bachelor degree in Electrical Engineering and Automation from Liaoning University of Petroleum and Chemical Technology, Liaoning, China in 2015. Then, he received his Master degree in Electrical Engineering from Arizona State University in 2018.

Sumit K. Mandal received B.Tech and M.Tech degree in Electronics and Communication from Indian Institute of Technology, Kharagpur, India in 2015. He is currently a Ph.D. student in Computer Engineering at the school of Electrical, Computer and Energy engineering, Arizona State University. He is a student member of the IEEE and ACM.

Umit Y. Ogras received his Ph.D. degree in Electrical and Computer Engineering from Carnegie Mellon University, Pittsburgh, PA, in 2007. From 2008 to 2013, he worked as a Research Scientist at the Strategic CAD Laboratories, Intel Corporation. He is currently an Associate Professor at the School of Electrical, Computer and Energy Engineering, Arizona State University.

Sule Ozev received her Ph.D. degree in Computer Science and Engineering from University of California, San Diego in 2002. Since then, she has worked as a member of faculty at Duke University and Arizona State University, where she is currently a professor. Her research interests include test optimization and built-in self-test for analog, RF, and hybrid devices, and modeling and optimization of hardware in cyber-physical systems.