

Review Notes 10/29/08

Note Title

10/29/2008

2MB Cache w 64 byte blocks

32-bit addresses

what area? 2MB - capacity, cache size

how many offset bits? $\log_2 \text{blk size} = \log_2 64 = 6$

how many tag bits? $32 - (6 + 15) = 11$

how many lines? How many index bits? $\log_2 (\text{number of lines}) = 15$

$$A = \underset{\text{lines}}{H} \times \underset{\text{blk size}}{W}$$

$$\equiv 2 \times 2^{20} = 2^6 \times H$$

$$H = 2 \times 2^{14} = 2^{15}$$

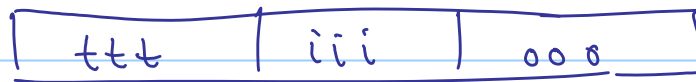
34 bit address

32 K lines

10 tag bits

9 offset bits = 512 byte blocks

What is capacity $2^9 \times 2^{15} = 2^{24}$



for Fully Assoc:

no index bits only tag and offset

Access time for L_1 cache 1 cycle

Miss rate of L_1 cache 5%

Miss penalty of L_1 cache 20

$$AMAT = 1 \text{ cycle} + 5\% \times 20^{\text{cycles}} = 2 \text{ cycles}$$

inputs		outputs	
		S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

↑ ↑
 XOR and

inputs			outputs	
Cin			C	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1