Administrivia

Note Title 10/22/2008

- Exam 2 10/31 — Review 10/29
- Following specifications for programs
- Commenting assembly programs

Caching - Direct-mapped caches

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- Memory Hierarchy - closer to the processor is
  - smaller
  - faster
  - more expensive
  - contain a subset of what is stored at the lower levels.

- Caches work because of locality - spatial and temporal

How is a cache organized?

- smaller and faster than the next layer down.
- data will have to move in and out of cache
- where does it reside when in the cache?
  - multiple answers depending on the type of cache.
  - simplest – Direct Mapped cache.

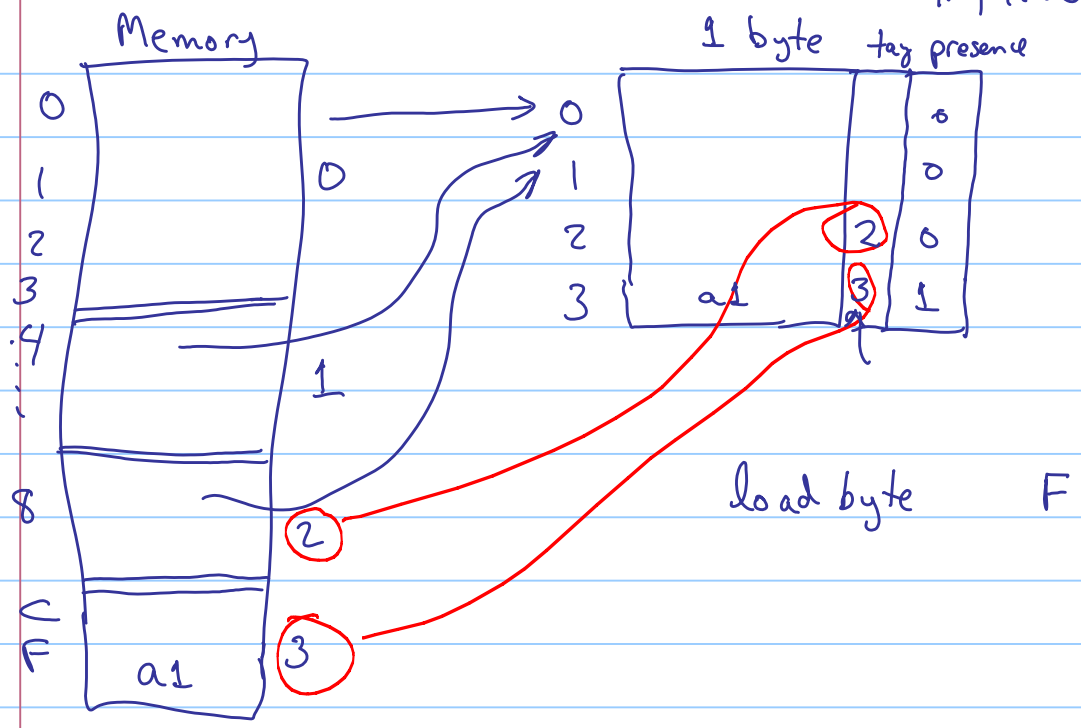
DMC

Each location in memory has a specific location in the cache where it is stored.

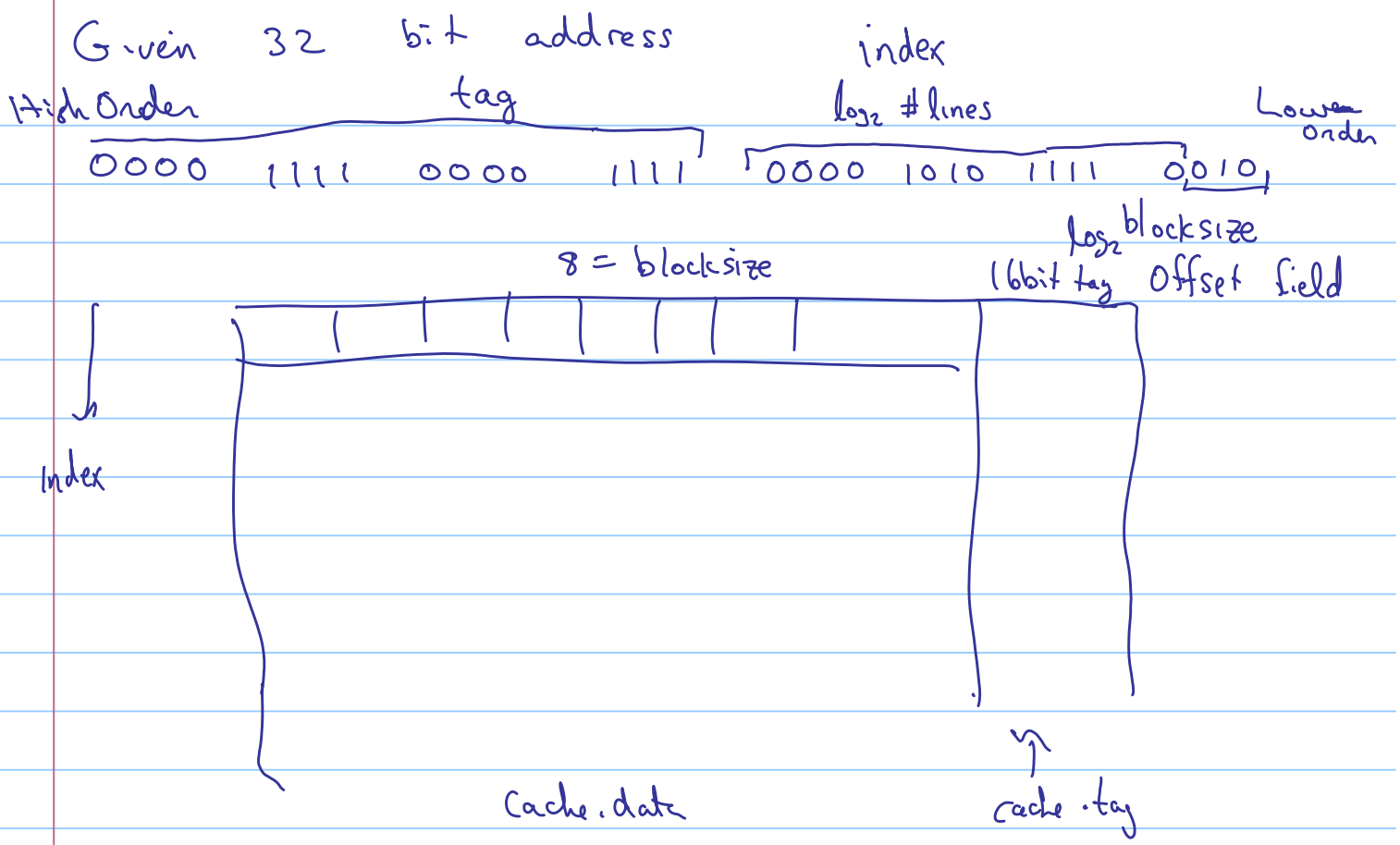
Total Size = Height x Width

# of lines

block size



Let's look at more realistic cache design.



32-bit addresses

Suppose we have 16 KByte cache w/
16 byte blocks.

How many bits in offset field? 4 bits
How many bits in the index field?
- How many lines? - 1024 lines - 10 bits
How many bits in the tag field? 18 bits

Steps in looking up an address in a DMC:
- break address into [tag, index, offset]
- compare cache.tag[index] to tag
  - if = return cache.data[index][offset]
  - if ≠ ...

if $

    Get rid of contents of cache [index]
    load cache [index] from memory [tag || index]