

Ch. 16 -

Device drivers - structure upper & lower half

open-read-write close paradigm

buffering

Q.

~~pipelining~~

Modern processor architecture - cell processor -

not so much what but why?

Forth -

difference betw. intel and MIPS architecture

translation of ^{conventions} push, pop, ~~copy~~ copy operations,
function calls, Variable access and manipulation

linked-list following - starting point ~~just~~ intel code +

close.asm.py - warning not everything is done correctly!

open book Button only; ~~about notes~~ whatever notes you
care to write in the book (!)

Ch 17 Parallelism

Kinds of parallelism micro vs macro, symmetric vs asymmetric

fine grain vs coarse grain, explicit vs implicit

SISD, SIMD, MIMD

techniques for communication / coordination; the problem of contention
MP performance.

Ch. 18 pipelining

concept; software;

how pipelines increase performance

~~the~~ performance of a pipeline - what limits it.

Ch. 19 - performance -

measures of performance - important principle - ^{measures what you} can do but ^{can do} benchmarks.

Cell process - goals; not so much what as why?

Review previous exams: ~~from~~ I will pull one or two ^{directly} problems from each of the ~~p~~ midterms.