Intro to the MIPS processor

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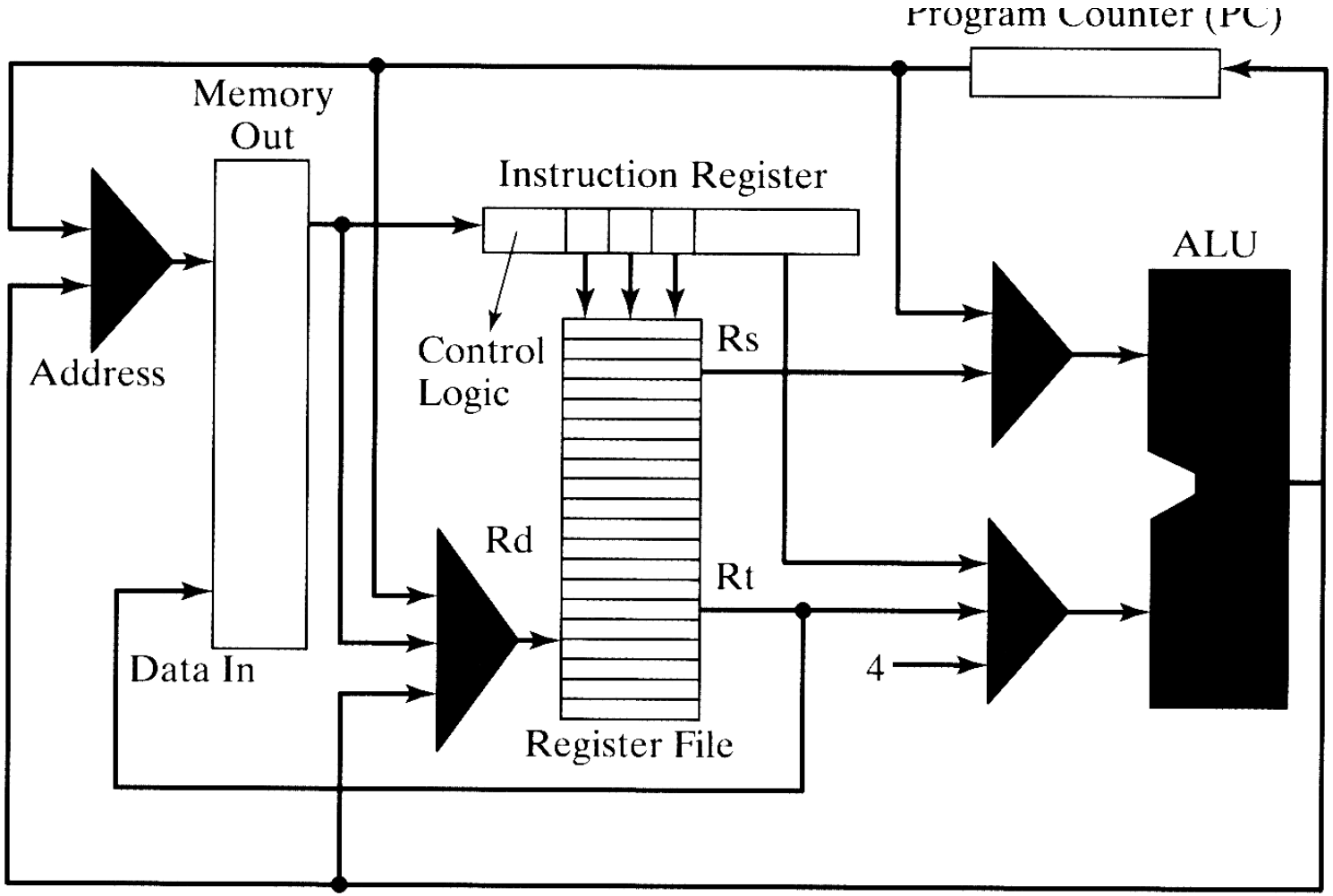
Datapath Diagram (Britton)



Register file

- Special purpose:
  - Number 0, $zero, always 0
  - Nr. 31, $ra, function return address
- General purpose:
  - Numbers 1-31
- Conventions for GP registers
  - Number 1, $at, assembler temporaries
  - Numbers 2&3, $v0, $v1, function returns vals
  - Numbers 4-7, $a0-$a3, function args

Register file (cont.)

- Conventions (cont.)
  - Nrs. 8-15, $t0-$t7, caller-save temps
  - Nrs. 16-23, $s0-$s7, callee-save temps
  - Nrs. 24-25, $t8-$t9, caller-save temps
  - Nrs. 26-27, $k0-$k1, reserved for OS
  - Nr. 28, $gp, globals pointer
  - Nr. 29, $sp, stack pointer
  - Nr. 30, $fp, frame pointer

Additional Registers

- Program counter/Instruction pointer
- Instruction register
- Status register
  - Condition codes
  - Interrupt masks
  - Processor operating state
  - …later
- Floating point registers
  - 32 32-bit or 16 64-bit

Memory

- Up to 4 GB (2^32-1)
- Word: 32 bits
- Half-word: 16 bits
- (Contrast with Intel terminology)

Instructions

- 6-bit op-code
- 27 bits depending on the op-code
- Register format
  - 2 operand source registers; 1 destination register; 6-bit function code; 5 unused bits
- Immediate format
  - 1 operand source; 1 destination; 16 bits *immediate* data
- Jump immediate instructions
  - 26-bit destination.
- Jump register instructions
  - 32-bit destination in a register

Load/Store Instructions

- Load/Store architecture – only operations accessing memory are load and store
- lw targetReg, offset(sourceReg)
  - Example: lw $s1,8($a0)
- sw sourceReg, offset(targetReg)
  - Example: sw $s1,12($a0)
- Offset is 16-bit signed
- Additional signed/unsiged byte/halfword load/store instructions

Fetch-execute cycle

- Instruction fetch: retrieve instruction at memory location specified by ip into instruction register; ip += 4
- Operand fetch: retrieve values from operand registers into ALU
- Execute: Perform the operation
- Write back: store result in register
- Modify for memory-access instructions