

Problem 1.

Consider two machines (Alpha and Beta) that have the following classes of instructions: Arithmetic and Logic integer instructions (AL), Load (Ld), Store (St), Branch (Br), Floating Point Add (FPadd), Floating Point Multiply (FPMult), and Floating Point Divide (FPdiv). Both machines have the **same** instruction set architecture. These machines execute a program that have the following instruction mix

AL: 33%	Ld: 27%	St: 9%	Br: 14.2%
FPadd: 10.5%	FPMult: 6%	FPdiv: 0.3%	

Machine Alpha has a clock rate of 3.0 GHz. For this machine instructions take the following number of cycles to be executed.

AL: 1	Ld: 2	St: 2	Br: 2
FPadd: 3	FPMult: 6	FPdiv: 30	

On the other hand, machine Beta has a clock rate of 3.8 GHz. For this machine instructions take the following number of cycles to be executed.

AL: 1	Ld: 3	St: 3	Br: 2
FPadd: 4	FPMult: 7	FPdiv: 33	

Please determine what machine is faster and by how much.

Problem 2.

A machine (with a clock rate is 4.1 GHz) executes 400 million instructions of a program. 56% of the instructions are arithmetic instructions that require 2 clock cycles to be executed, 32% are branches and 12% are memory references (either loads or stores). Branch and memory reference instructions take 3 cycles to be executed.

- Consider an improvement for this machine, the number of cycles that are needed to execute a branch can be reduced depending on the branch decision. If a branch is taken, the machine needs 3 cycles as before. However, if the branch is not taken the machine needs only two cycles to execute the branch. In this program, 54% of the branches are taken. Please determine the impact (i.e. speedup) of the improvement.
- Let us have an additional improvement. We incorporate a buffer that helps to reduce the number of cycles needed to execute store instructions (which comprise 33% of the memory references). Now, store instructions take 2 cycles. With these two improvements (in a and b) what is the speedup in comparison with the original machine.