EE 334 COMPUTER ARCHITECTURE Spring 2008

Sloan 5 M,W,F 9:10-10AM

Objectives: To provide a sound background on computer architecture. The main focus is processor design and evaluation with case studies. A number of architectural alternatives are described and evaluated using quantitative approaches. Pre-requisite: EE234 (EE314)

1. Computer Abstractions and Technology ***(Chapter 1)***

1.1 Programs
1.2 Integrated circuits
1.3 Microprocessors

2. Instruction Set Architecture ***(Chapter 2)***

2.1 Instruction types: Arithmetic, Logic, Branch, Memory
2.2 Operand storage, type and size
2.3 Examples of instruction sets (MIPS and DLX)

3. Computer Arithmetic ***(Chapter 3***

3.1 Number representation
3.2 Addition/Subtraction
3.3 ALU
3.4 Multiplication/Division
3.5 Floating Point

4. Performance Issues ***(Chapter 4)***

4.1 Metrics
4.2 Benchmark Programs
4.3 SPEC Benchmarks

5. Processor's Datapath ***(Chapter 5)***

5.1 Building a Datapath
5.2 Implementation issues
5.3 Pentium Pro Implementation

6. Pipelining ***(Chapter 6)***

6.1 Pipelining principle
6.2 Pipelined datapth
6.3 Data Hazards and forwarding
6.4 Branch Hazards
6.5 PowerPC 604

7. Memory Hierarchy ***(Chapter 7)***

7.1 Principle of locality
7.2 Memory hierarchy
7.3 Cache memory
7.4 Virtual Memory

Textbook: D. A. Patterson and J. L. Hennessy, *Computer Organization and Design: The Hardware/Software Interface,* **Third Edition**. Morgan Kaufmann Publishers, 2005.

Instructor: Dr. José Delgado-Frias
Email: jdelgado@eecs.wsu.edu
Office: EME 102D
Phone: (509)335-1156

Office Hours: Wednesday 10:30am – 12noon (or by appointment.)