

Problem 1.

[25 points]

A program is run on a load and store processor that has a clock cycle time of $0.2nsec$. The instruction mix is given below.

Instruction type	Executed instructions	Multi-cycle CPIi	Pipeline CPIi
ALU	9.3×10^8	4	1
Load	8.1×10^8	5	1
Store	4.3×10^8	4	1
FP inst.	1.2×10^8	6.8	4.8
Branch	3.4×10^8	3	2

Please determine:

a) The CPI for each implementation.

b) What implementation is faster and by how much.

Problem 2.

[40 points]

A benchmark in a five-stage pipelined processor has the following characteristics:

26% ALU instructions,

23% load instructions

14% of the loads are followed by instructions that use the data being loaded.

25% of these loads are followed by stores. Let us assume that the destination register for load instruction is R_y . The store instructions that have dependencies on the loads:

o 40% of the stores have the form: **SW R_y , 0(R_x)**

o 60% of the stores have the form: **SW R_x , 0(R_y)**

14% store instructions

19% floating point instructions, and

18% branch instructions (54% of these branches are taken).

This processor's CPI_{int} and CPI_{FP} are equal to 1 and 3.1, respectively (when there are no hazards). Please answer the following questions:

a) Assuming that all the branch instructions cause hazards (the penalty is 1 clock cycle), please compute the overall CPI.

b) If the branch delay slot is scheduled using the three strategies and NO-OP as follows:

Delay Slot	NO-OP	Fall through	Target	Before
%	44%	11%	23%	22%

Please determine the new CPI

[35 points]

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foo:    LW      R10,0(R1)
        MULT   R4,R3,R10
        LW      R6,0(R2)
        ADD     R6,R4,R6
        SW      R6,0(R2)
        SUBI    R3,R1,#512
        ADDI    R1,R1,#8
        ADDI    R2,R2,#8
        BNZ     R3,foo
```

- [illegible]

- [illegible]