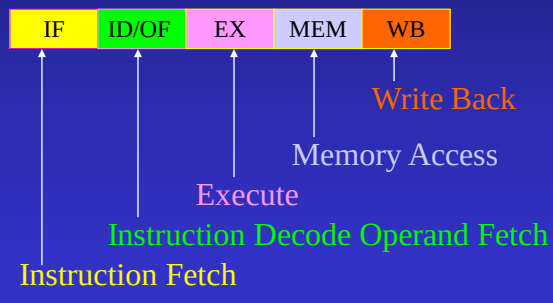
Chapter 4
(Part B)

PIPELINING

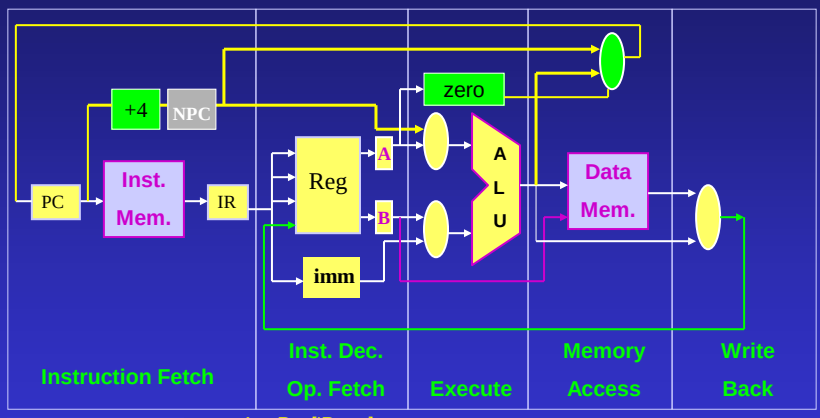
Processor

Basic steps to process an instruction



2

Datapath



IR ← Mem[PC]

NPC ← PC + 4

A← Reg[IR $_{6..10}$]

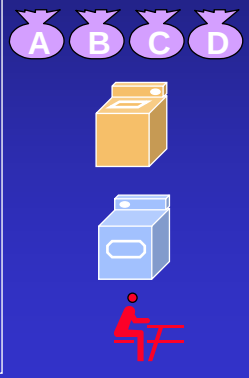
B← Reg[IR $_{11..15}$]

Imm← ((IR$_{16}$)^{16}## IR $_{11..15}$]

3

Pipelining: Its Natural!

- Laundry Example
- Ann, Brian, Cathy, Dave each have one load of clothes to wash, dry, and fold
- Washer takes 30 minutes
- Dryer takes 40 minutes
- "Folder" takes 20 minutes



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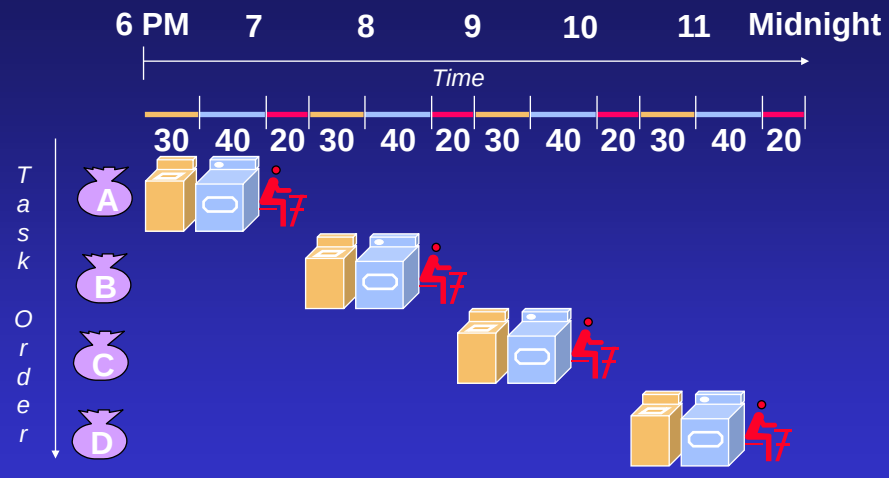
Sequential Laundry



- Sequential laundry takes 6 hours for 4 loads
- If they learned pipelining, how long would laundry take?

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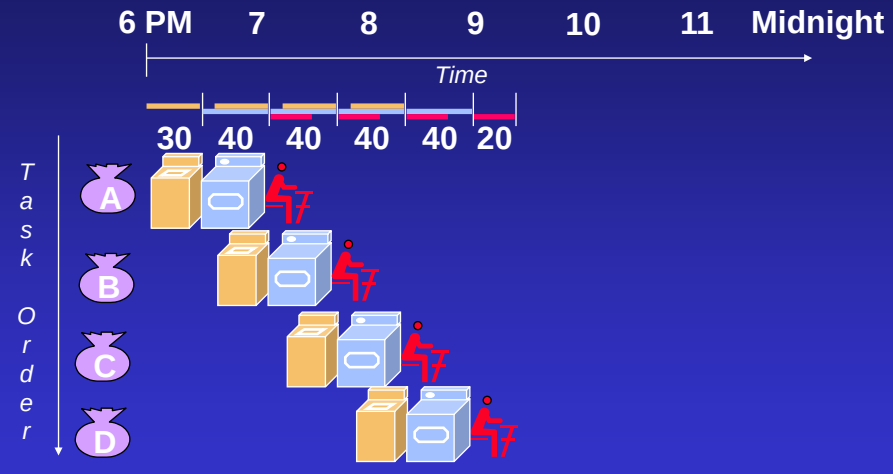
Pipelined Laundry
Start work ASAP



- Pipelined laundry takes 3.5 hours for 4 loads

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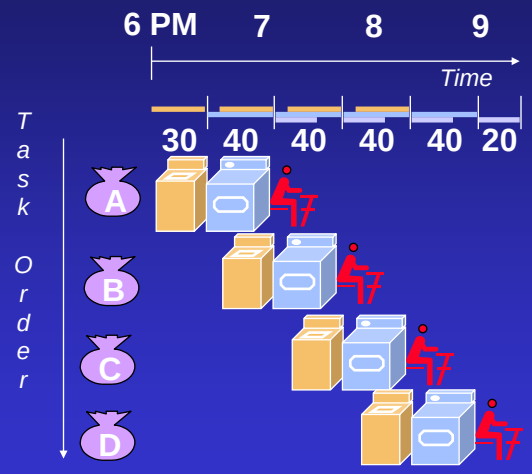
Pipelining Lessons



- Pipelining doesn't help latency of single task, it helps throughput of entire workload
- Pipeline rate limited by slowest pipeline stage
- Multiple tasks operating simultaneously
- Potential speedup = Number pipe stages
- Unbalanced lengths of pipe stages reduces speedup
- Time to "fill" pipeline and time to "drain" it reduces speedup

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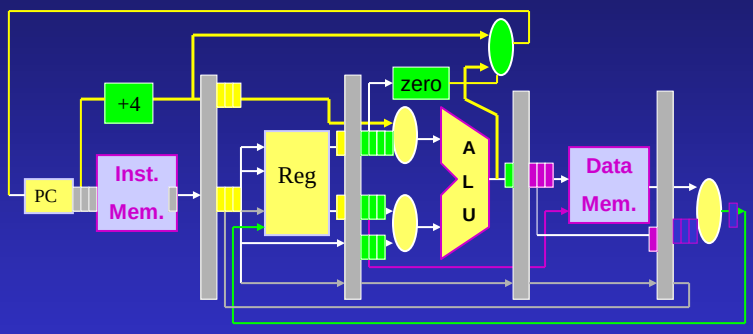
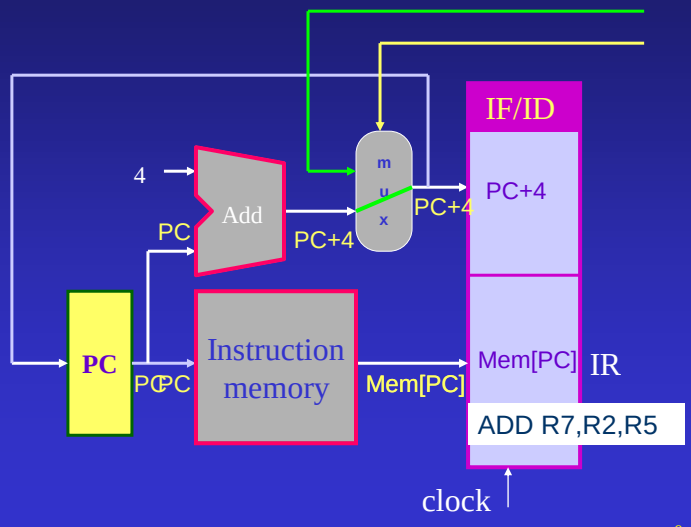
Datapath w/ pipeline



8

0

Instruction Fetch (IF) stage



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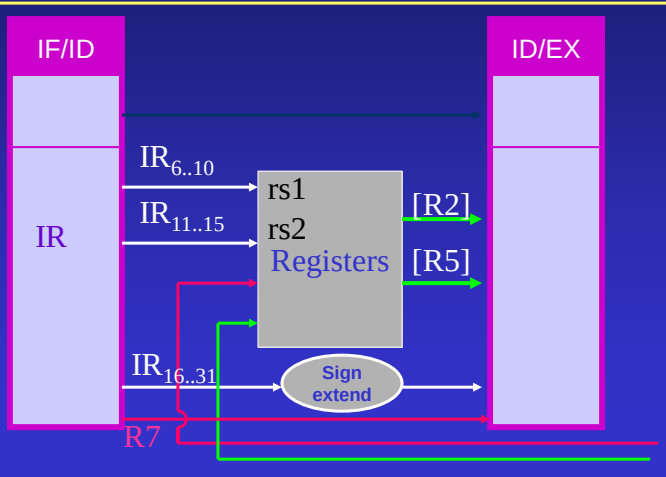
1

Instruction Decode (ID) stage



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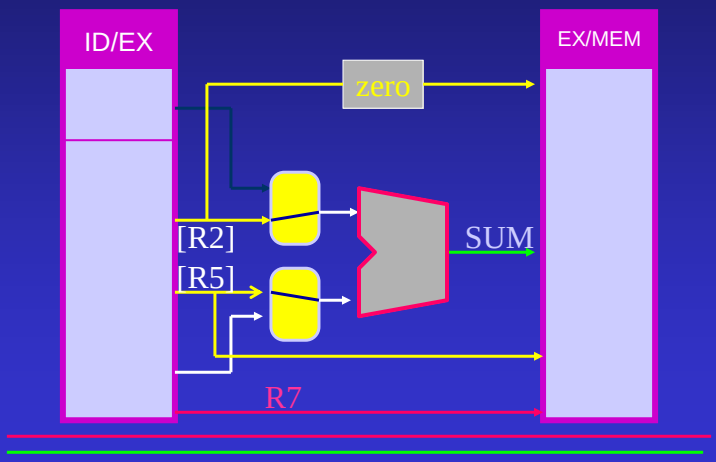
2

Execution (EX) stage



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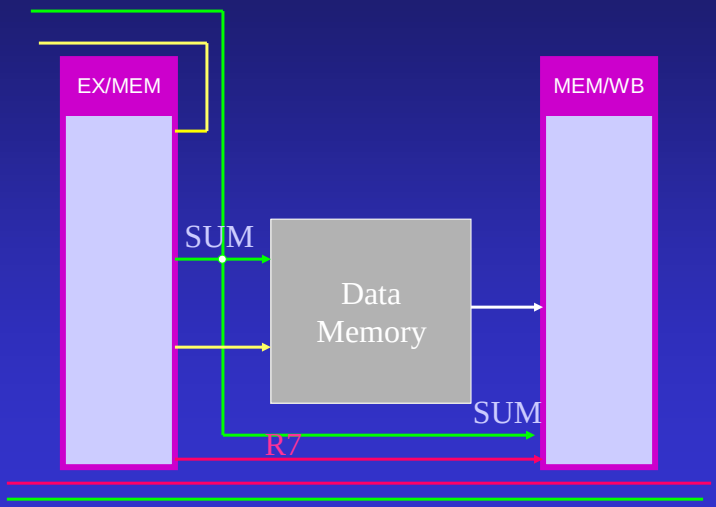
3

Memory (MEM) stage



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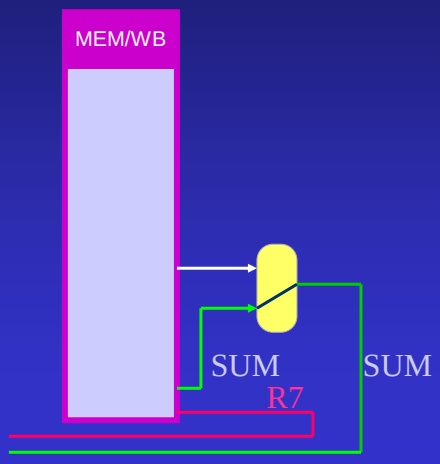
4

Write Back (WB) stage



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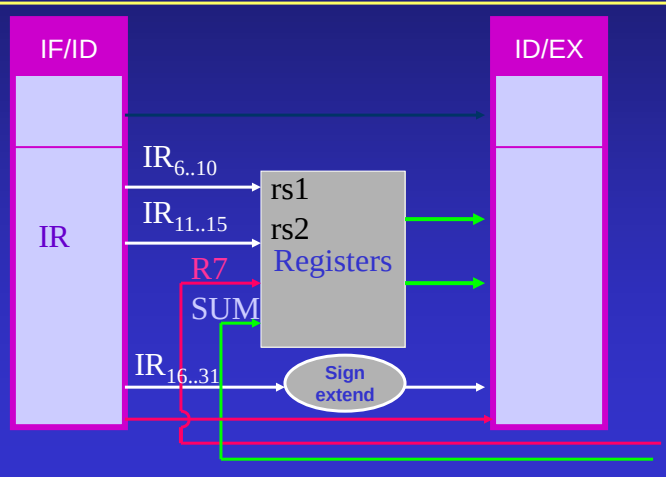
4

Instruction Decode (ID) stage



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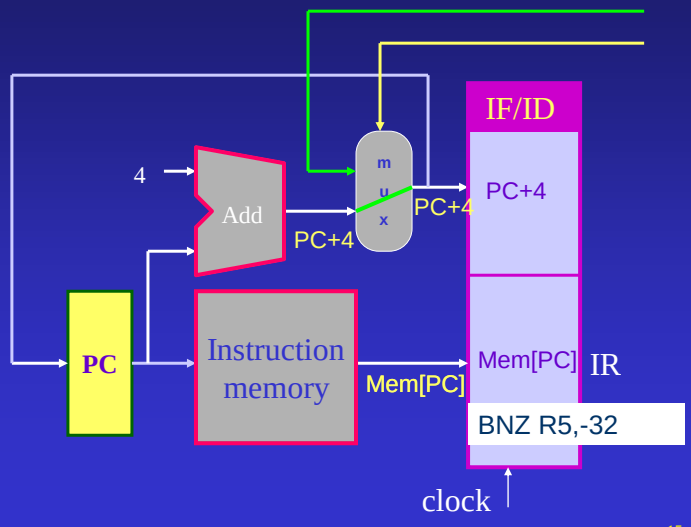
100

Instruction Fetch (IF) stage



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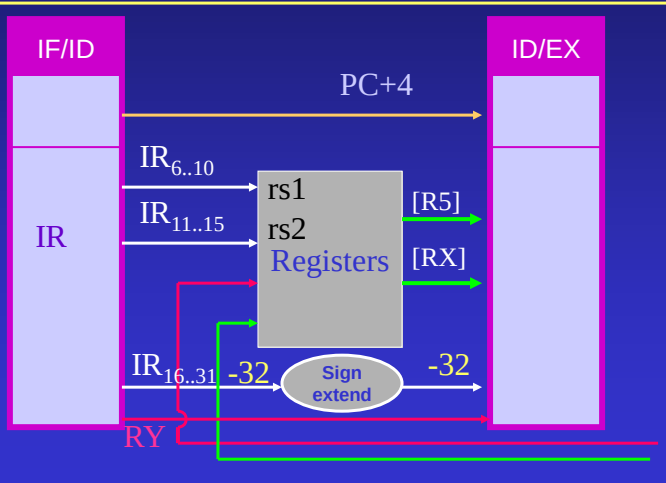
101

Instruction Decode (ID) stage



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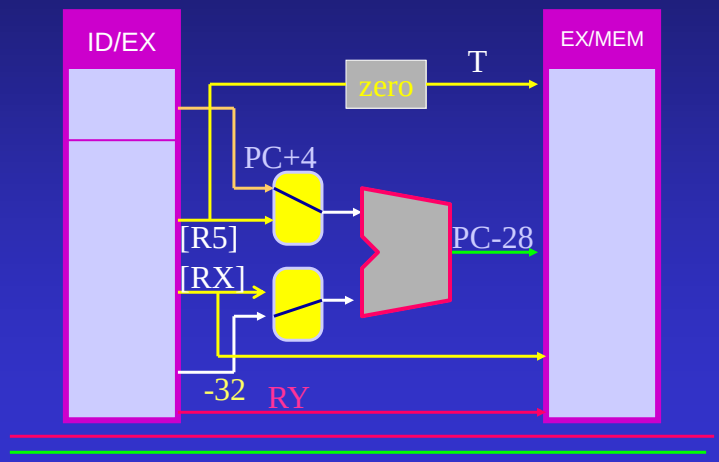
102

Execution (EX) stage



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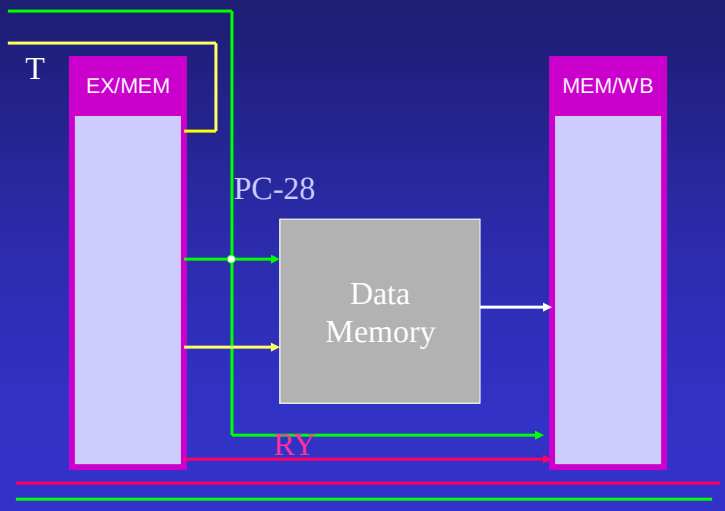
Memory (MEM) stage



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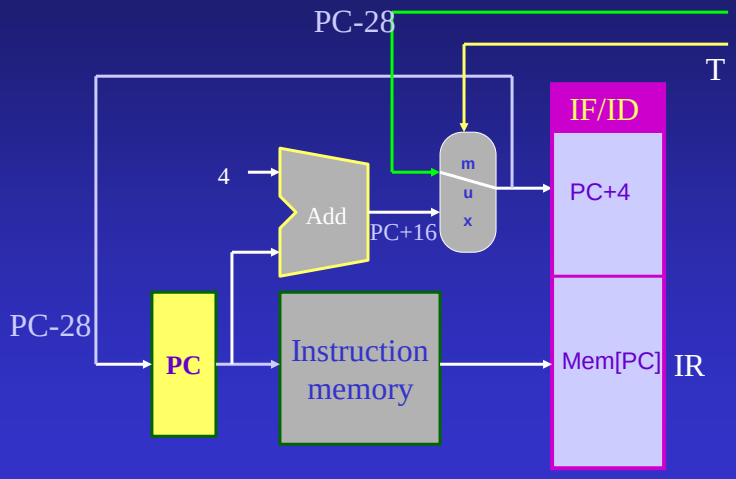
Instruction Fetch (IF) stage



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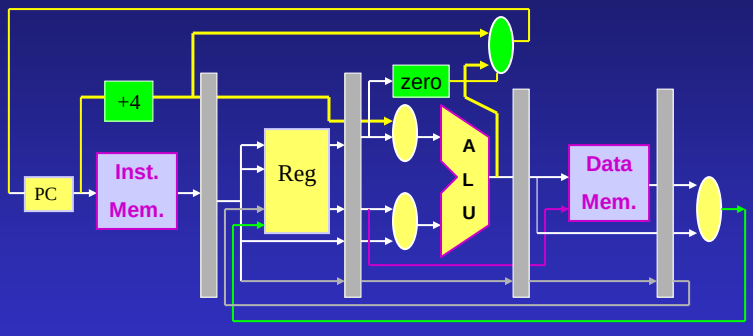
Datapath w/ pipeline



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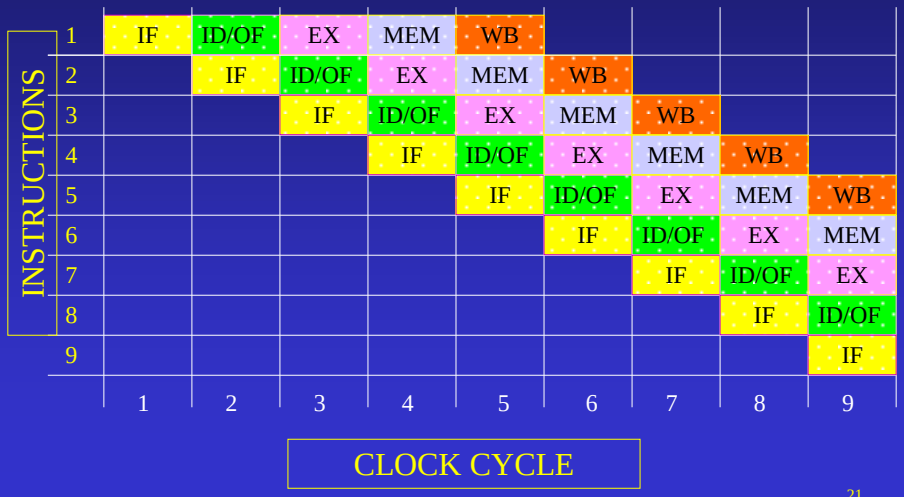
Pipeline



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Pipeline Hazards

- Structural Hazards
  - two or more instructions use same hardware at the same time.
- Data Hazards
  - Data dependencies
  - Result from inst. j is needed by inst. k
- Control Hazards
  - Branch changes flow, what happen with the following instruction(s)

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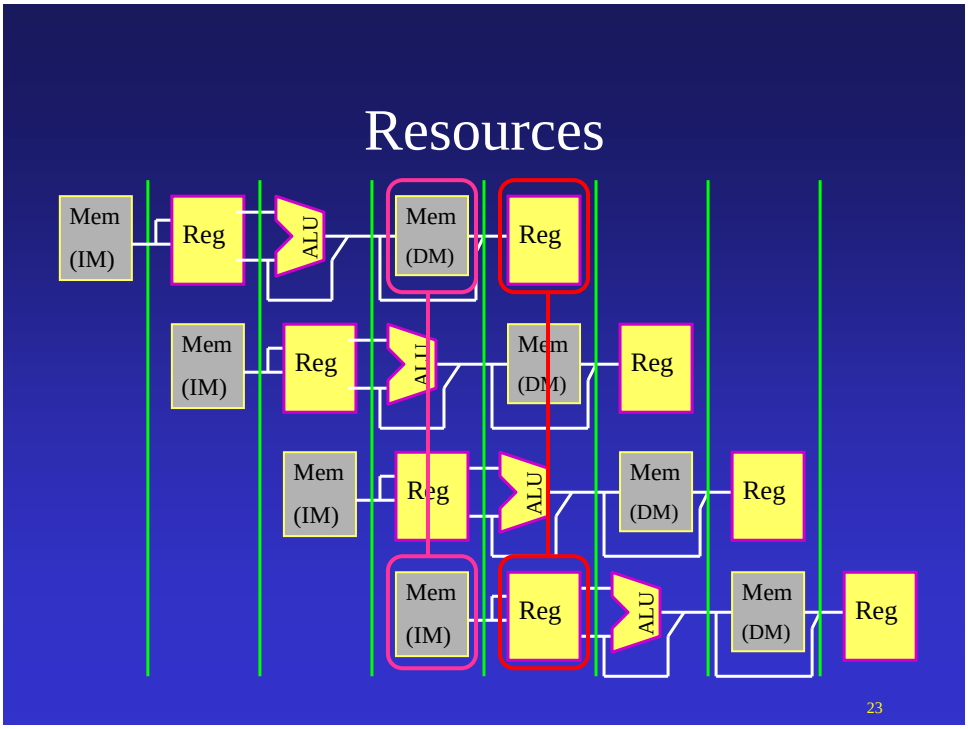
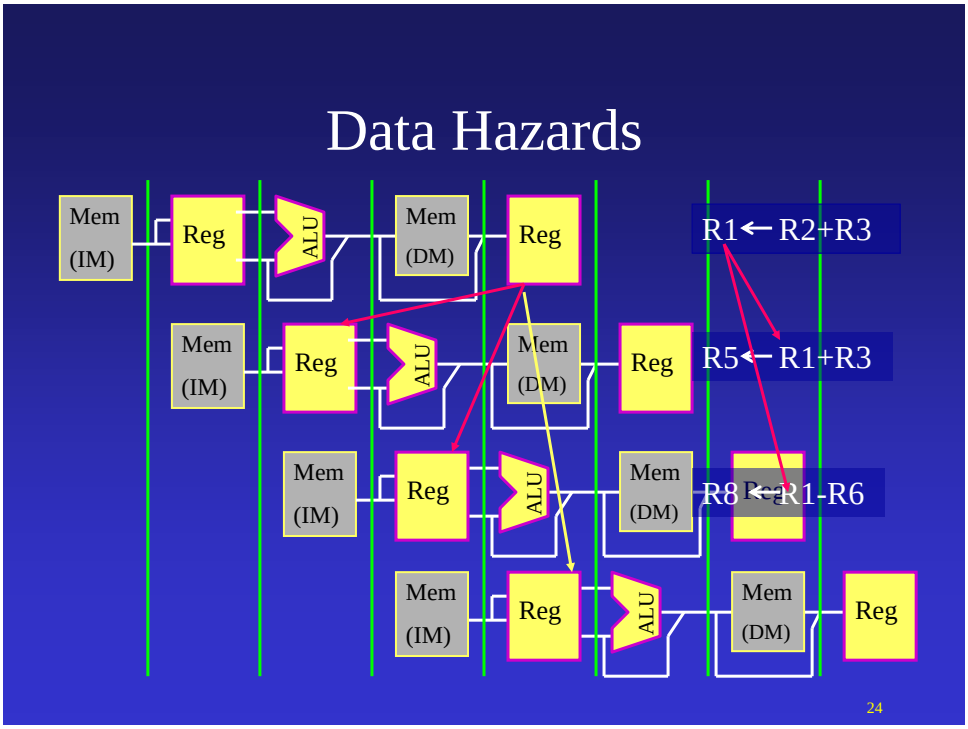

Resources
Mem (IM)
Reg
ALU
Mem (DM)
Reg
23


Data Hazards
Mem (IM)
Reg
ALU
Mem (DM)
Reg
R1← R2+R3
R5← R1+R3
R8← R1-R6
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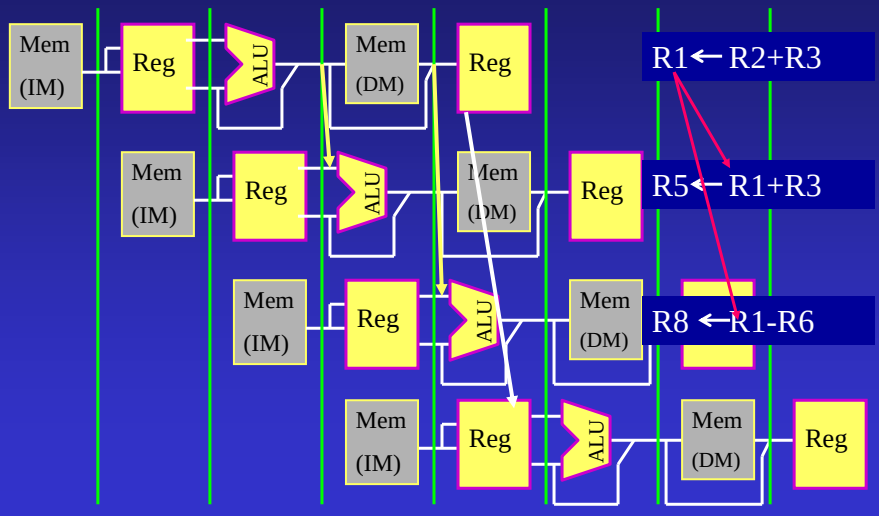
Data Forwarding



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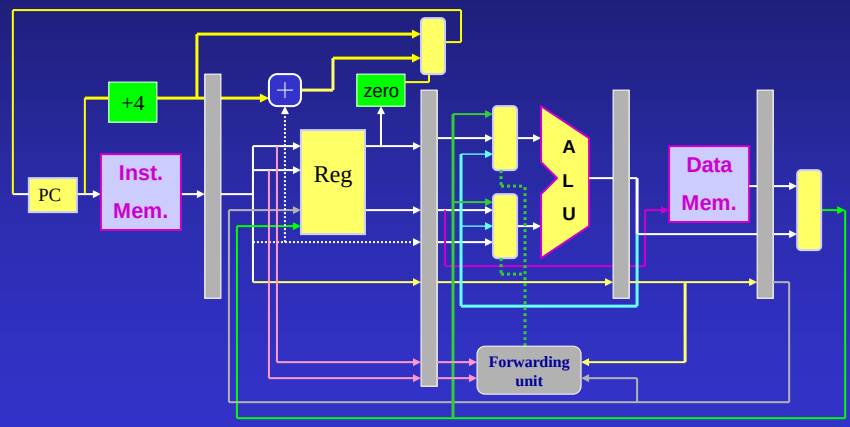
Datapath w/ pipeline



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Example

ADD R1,R2,R3

SUB R4,R3,R1

XOR R7,R8,R1

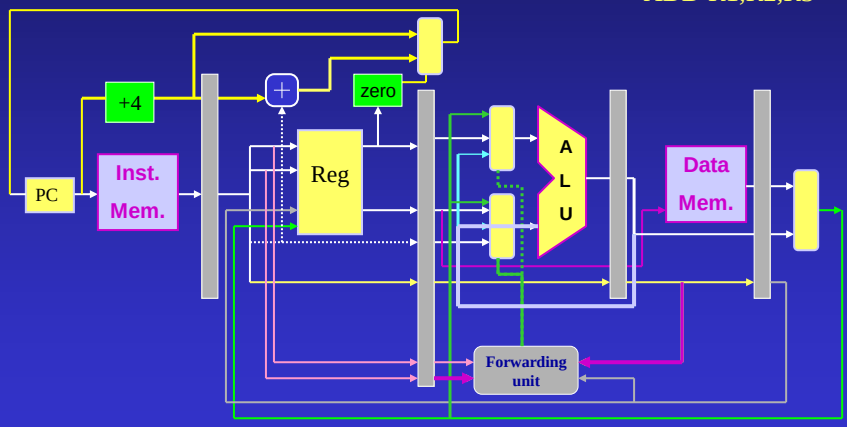
ADD R1,R2,R3

SUB R4,R3,R1

XOR R7,R8,R1

ADD R1,R2,R3

ADD R1,R2,R3



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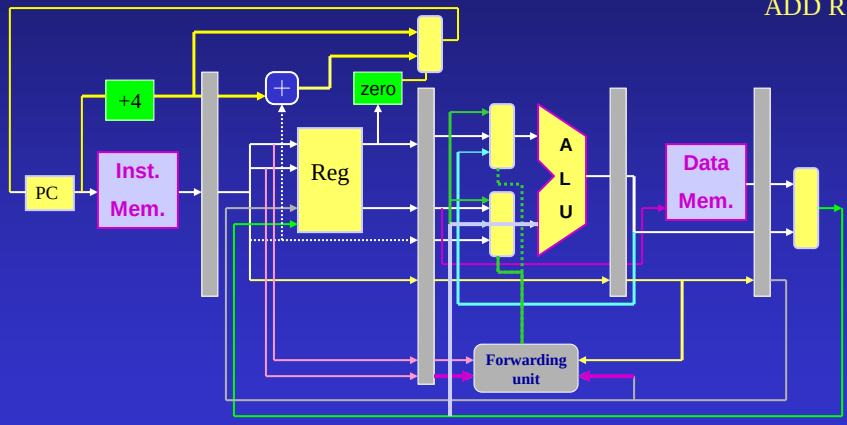
Example

XOR R7,R8,R1 SUB R4,R3,R1

ADD R1..



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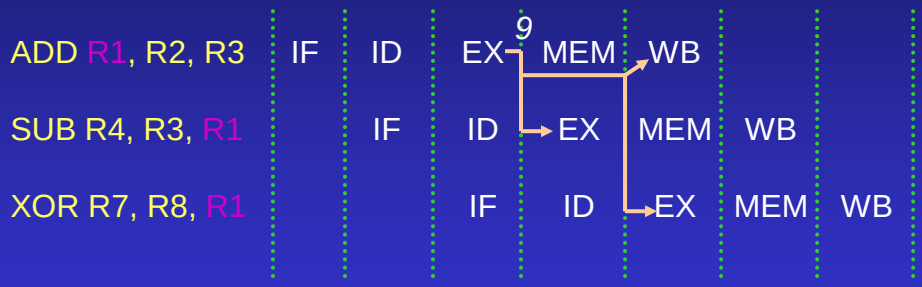
Assume R2 & R3 values are 7&2

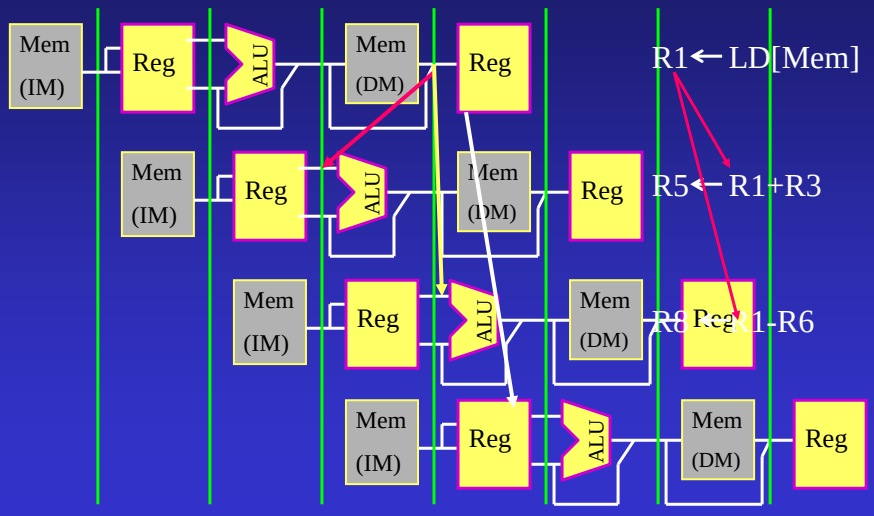


Data Hazard Classification

- RAW (Read After Write)
  - **w/ forward only load presents a problem**
- WAW
- WAR
- RAR

j:	R1 ←
k:	RY ← R1
j:	R1 ←
k:	R1 ←
j:	← R1
k:	R1 ←
j:	← R1
k:	← R1

Data Forwarding (load)



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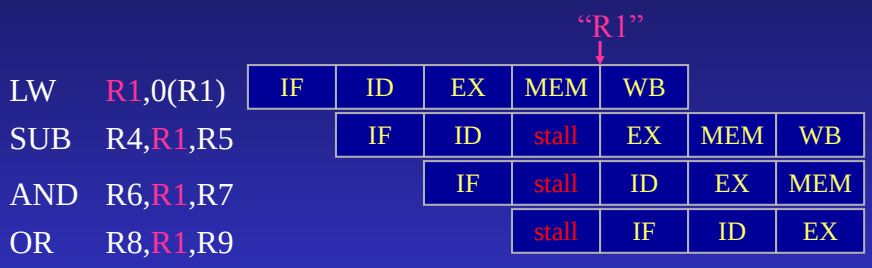
Data hazard (load)



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Branch

```
          BR  R1, LABEL_A
          ADD R2,R3,R7
          AND  R5,R7,R11
          :
          :
LABEL_A:  LD  R4,R2,005
```

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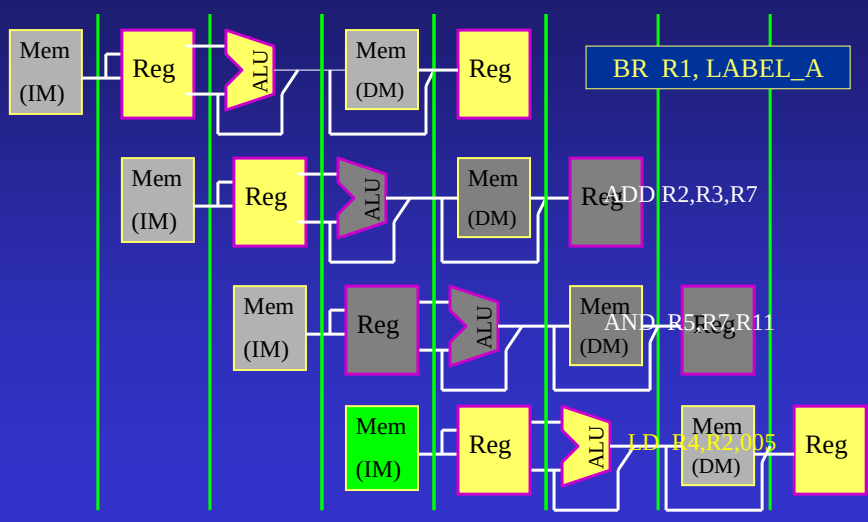
Branch



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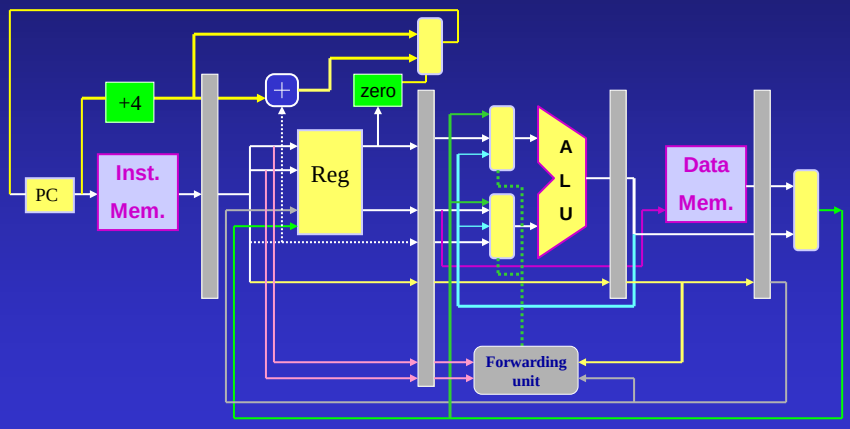
Datapath w/ pipeline



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What to do w/ branch

- Reduce the number of cycles to decide on a branch.
- Delayed branch (Software Solutions)
  - NO-OP
  - move instructions
    - from before
    - from target
    - from fall through

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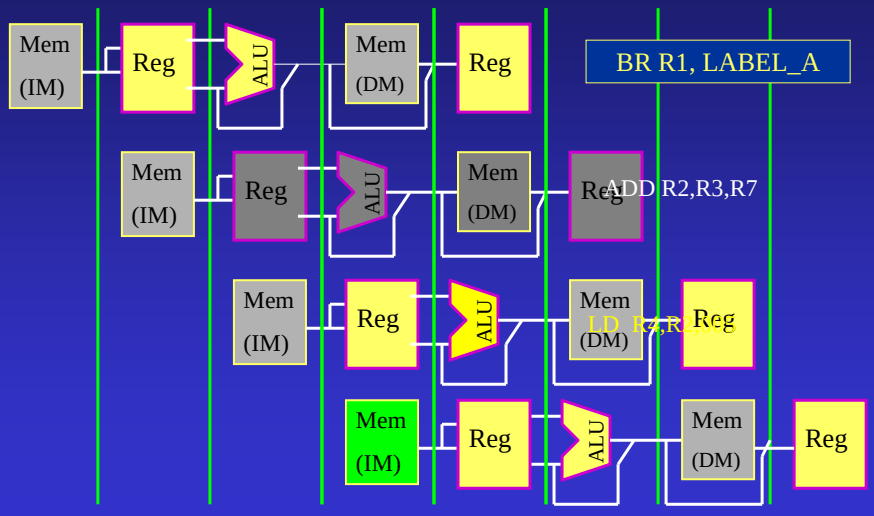
Branch



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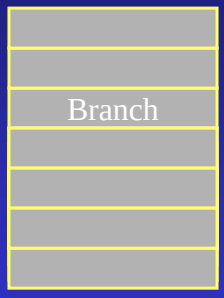
NO-OP



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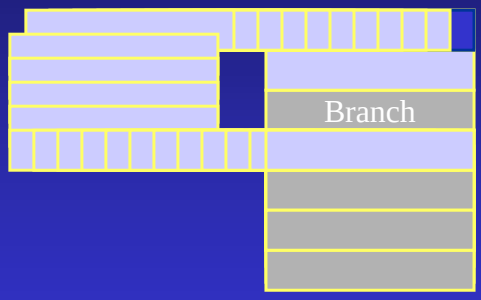
From Before



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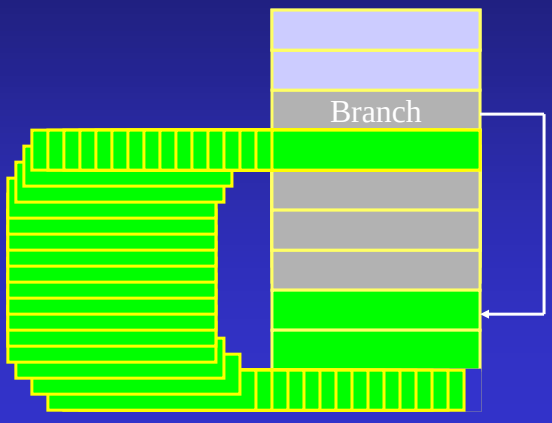
From Target



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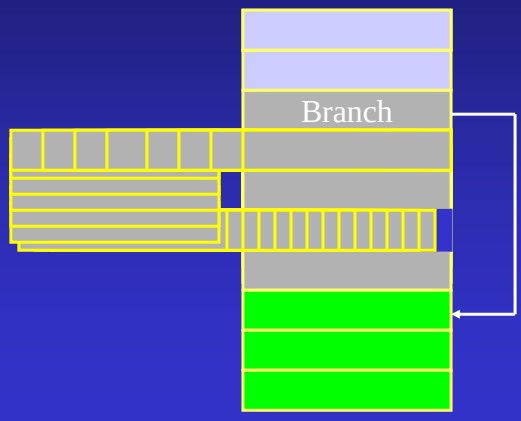
From Fall Through



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Example

loop:	LW	$1,0($2)	R1 ← MEM[R2+0]
	ADDI	$1,$1, 1	R1 ← R1+1
	SW	$1,0($2)	MEM[R2+0] ← R1
	ADDI	$2,$2,4	R2 ← R2+4
	SUB	$4,$3,$2	R4 ← R3-R2
	BNEZ	$4,loop	IF R4 ≠ 0 GOTO loop

Initial value: R3 = R2+396

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