E E 3 3 4
COMPUTER ARCHITECTURE

School of Electrical Engineering and Computer Science

WASHINGTON STATE UNIVERSITY

Topics

1. Computer Abstractions and Technology ***(Chapter 1)***

1.1 Programs

1.2 Integrated circuits

1.3 Microprocessors

2. Instruction Set Architecture ***(Chapter 2)***

2.1 Instruction types: Arithmetic, Logic, Branch, Memory

2.2 Operand storage, type and size

2.3 Examples of instruction sets (MIPS)

3. Computer Arithmetic ***(Chapter 3)***

3.1 Number representation

3.2 Addition/Subtraction

3.3 ALU

3.4 Multiplication/Division

3.5 Floating Point

Topics (Cont'd)

4. Processor Architecture ***(Chapter 4)***

- 4.1 Building a Datapath
- 4.2 Pipelining principle
- 4.3 Pipelined datapth and control
- 4.4 Data hazards and forwarding
- 4.5 Control (branch) Hazards
- 4.6 Instruction-level parallelism
- 4.7 AMD Opteron X4

Topics (Cont’d)

5. Memory Hierarchy ***(Chapter 5)***

5.1 Principle of locality

5.2 Memory hierarchy

5.3 Cache memory

5.4 Virtual Memory

6. Multicore and Multiprocessor ***(Chapter 7)***

6.1 Parallel Processing

6.2 Share Memory Multiprocessors

6.3 Hardware Multithreading

6.4 Message passing multiprocessors

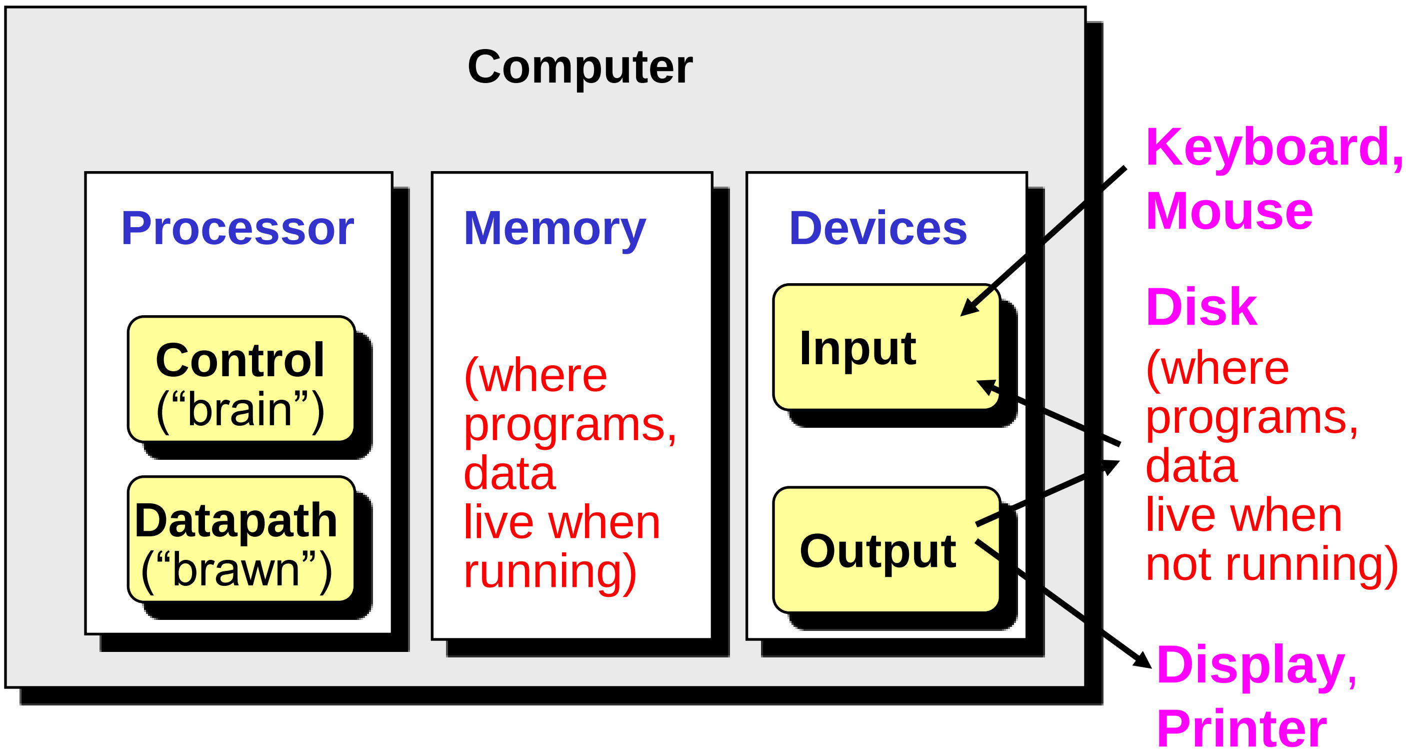
Textbook

D. A. Patterson and J. L. Hennessy,

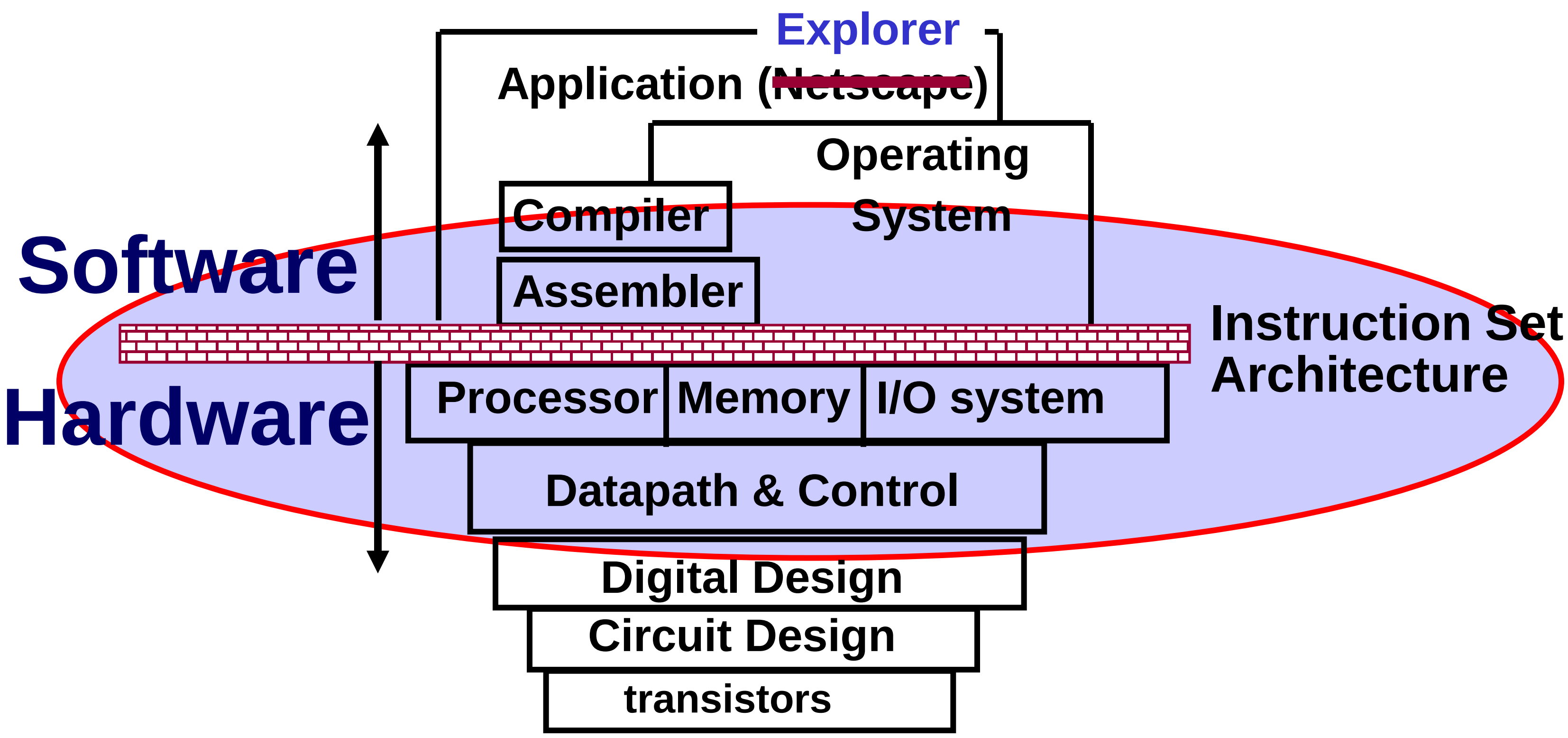
Computer Organization and Design: The Hardware/Software Interface,

Fourth Edition. Morgan Kaufmann Publishers, 2009.

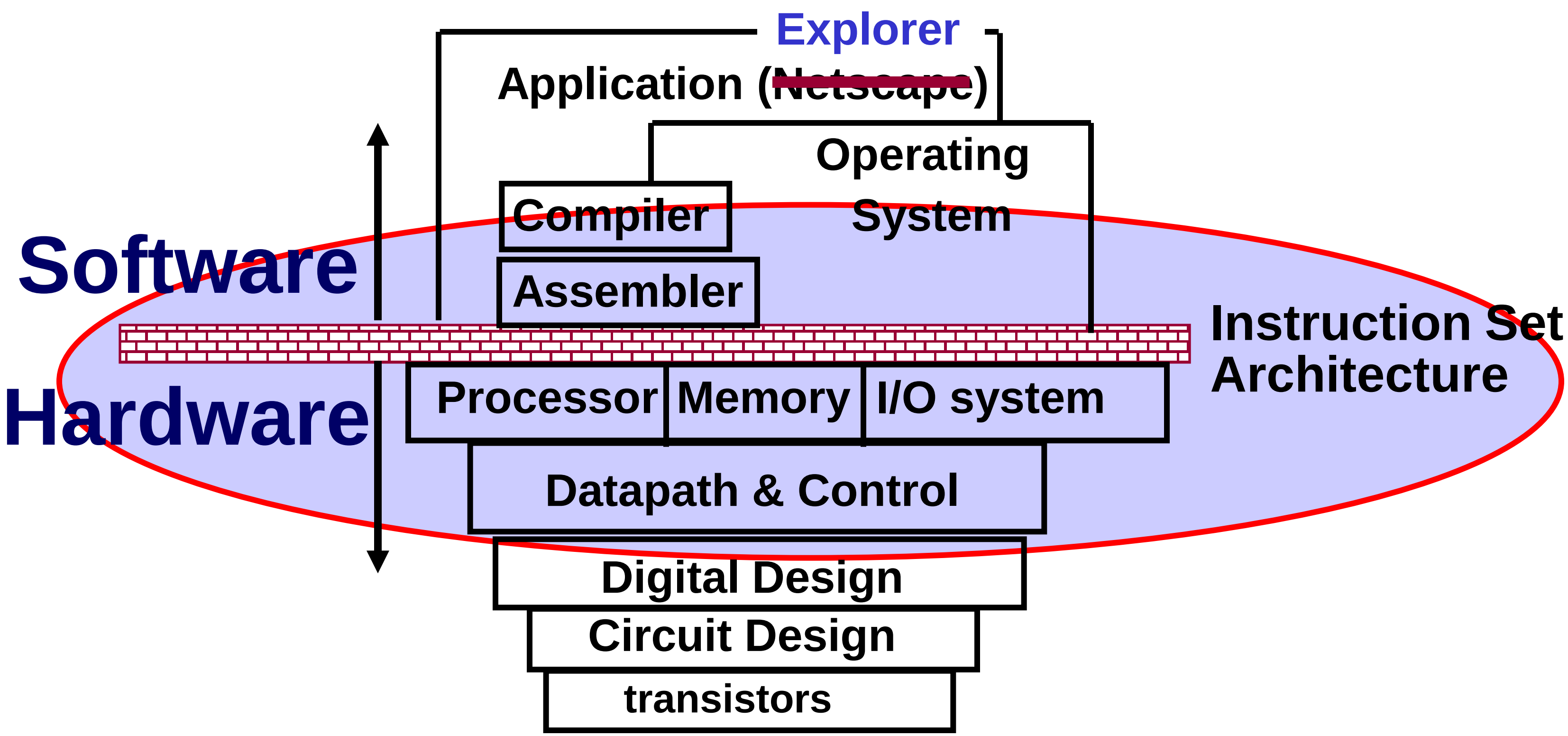
Basic components



Computer System



Computer System



Abstraction

- Delving into the depths reveals more information

- An abstraction omits unneeded detail, helps us cope with complexity

What are some of the details that appear in these familiar abstractions?

High-level language program (in C)

```
swap(int v[], int k)
{int temp;
   temp = v[k];
   v[k] = v[k+1];
   v[k+1] = temp;
}
```

C compiler

Assembly language program (for MIPS)

```
swap:
      muli $2, $5,4
      add  $2, $4,$2
      lw   $15, 0($2)
      lw   $16, 4($2)
      sw   $16, 0($2)
      sw   $15, 4($2)
      jr   $31
```

Assembler

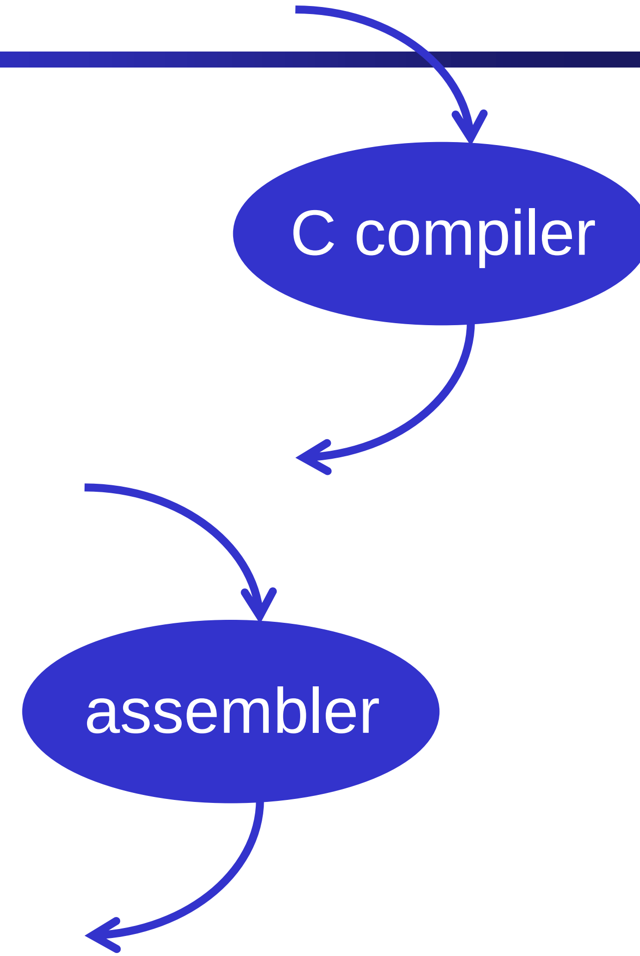
Binary machine language program (for MIPS)

```
00000000101000010000000000011000
00000000100011100001100000100001
10001100011000100000000000000000
10001100111100100000000000000100
1010110011110010000000000000000
                                00
 10101100011000100000000000000100
 00000011111000000000000000001000
```

Below the program

- High-level language program (in C)

```
swap (int v[], int k)
(int temp;
      temp = v[k];
      v[k] = v[k+1];
      v[k+1] = temp;
)
```



- Assembly language program (MIPS)

```
swap: sll   $2, $5, 2
      add   $2, $4,$2
      lw    $15, 0($2)
      lw    $16, 4($2)
      sw    $16, 0($2)
      sw    $15, 4($2)
      jr    $31
```

- Machine (object) code (MIPS)

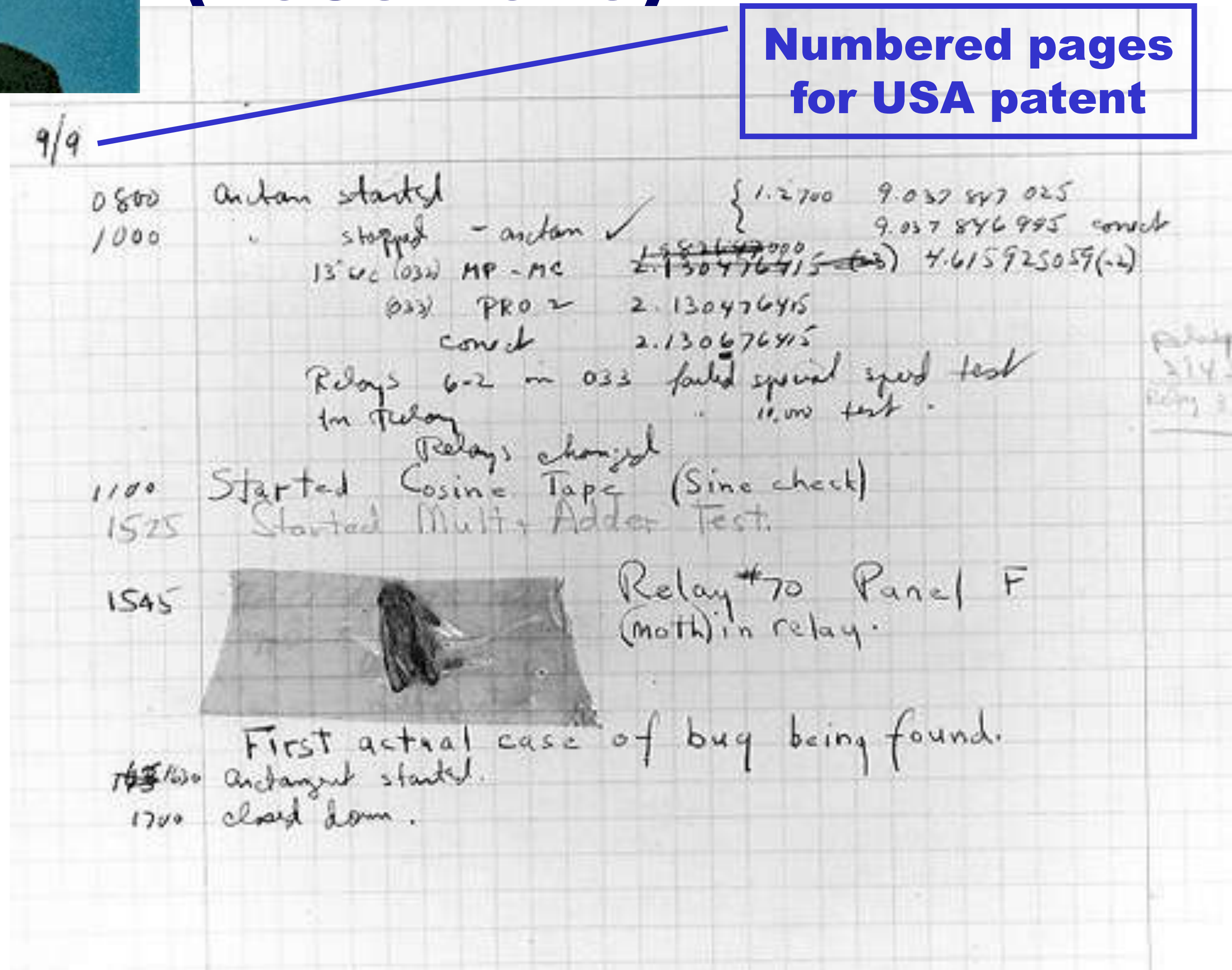
```
000000 00000 00101 0001000010000000
000000 00100 00010 0001000000100000
. . .
```

Computer history

Generation -1:	The early days	????-1642
Generation 0:	Mechanical	1642-1935
Generation 1:	Electromechanical	1935-1945
Generation 2:	Vacuum tubes	1945-1955
Generation 3:	Discrete transistors	1955-1965
Generation 4:	Integrated circuits	1965-1980
Generation 5:	VLSI	1980-????

Generation 1: Electromechanical (1935-1945)

Numbered pages for USA patent

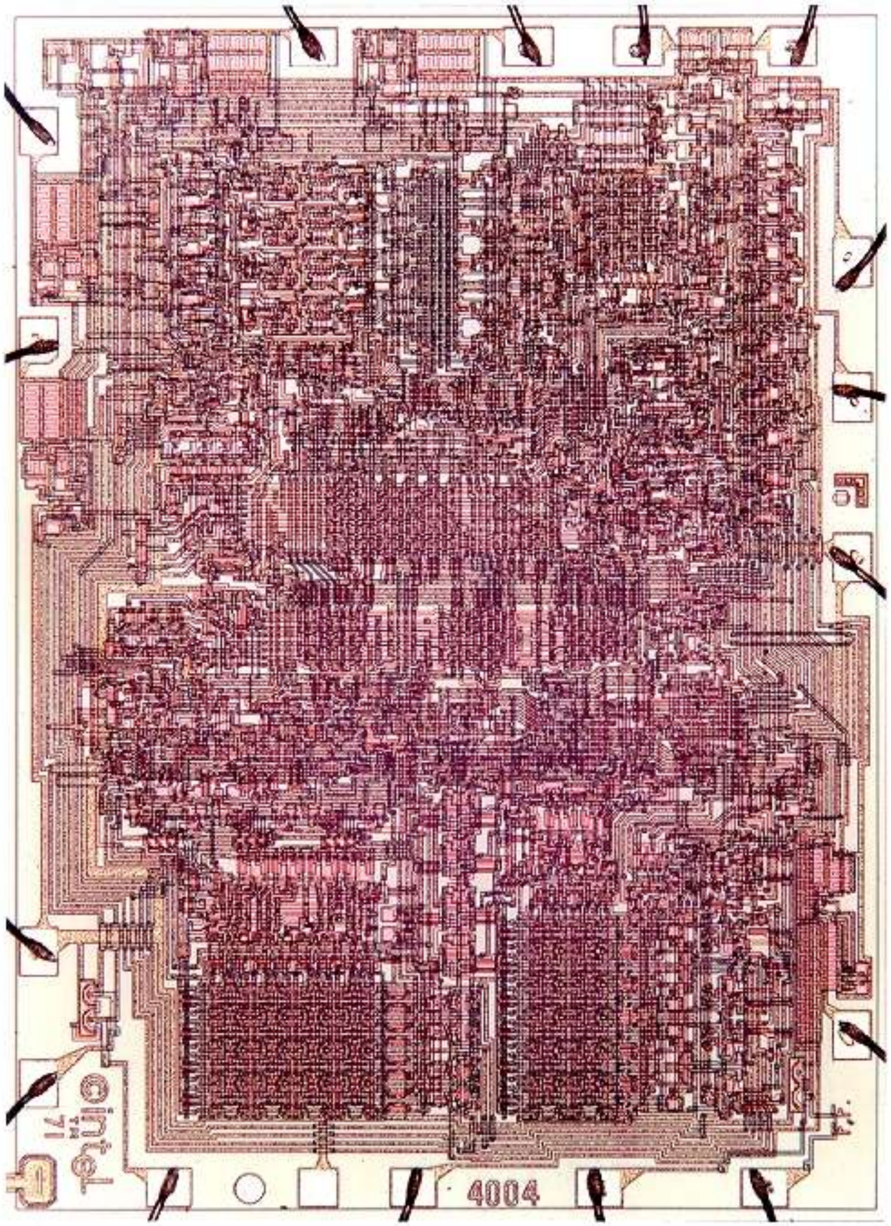


- Grace Murray Hopper found the first computer bug beaten to death in the jaws of a relay. She glued it into the logbook of the computer and thereafter when the machine stopped (frequently) she told Howard Aiken that they were "debugging" the computer.

Integrated Circuits

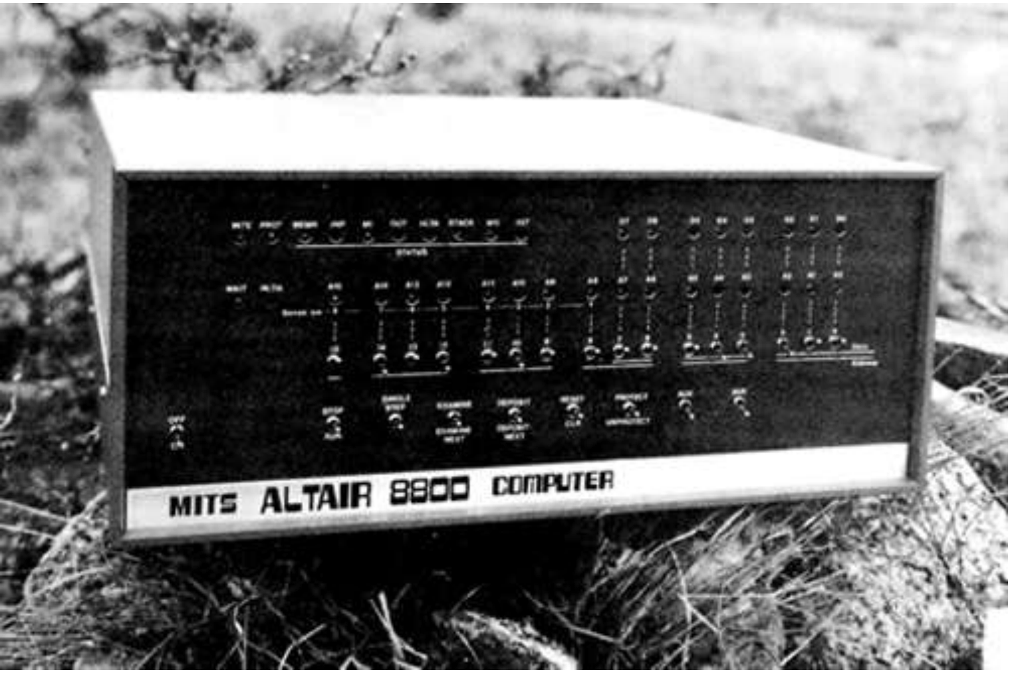
- Rapidly changing field:
  - vacuum tube → transistor → IC → VLSI
  - doubling every 1.5 years:
    memory capacity
    processor speed
    - *(Due to advances in technology <u>and</u> organization)*

Intel 4004



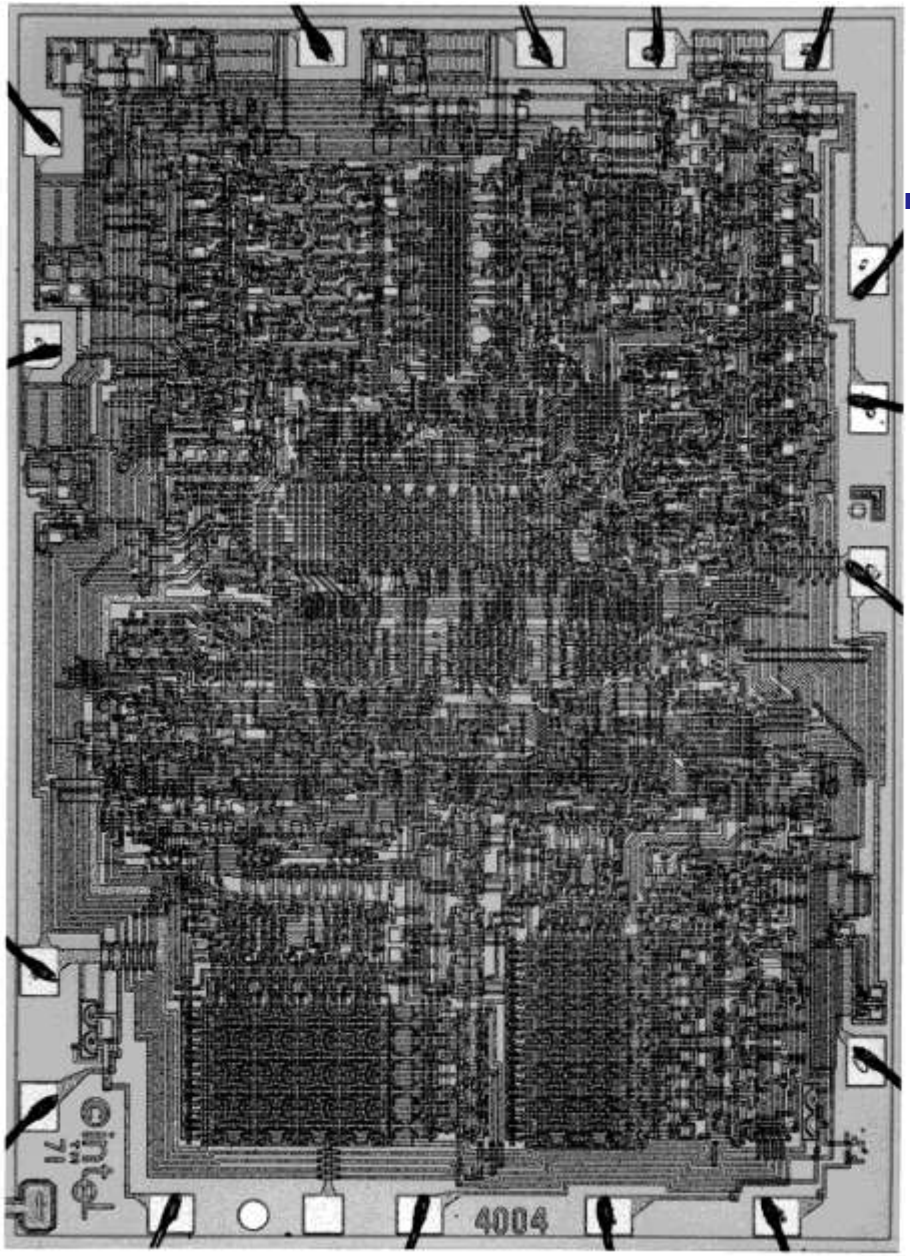
- In 1971, Ted Hoff produced the Intel 4004 in response to the request from a Japanese company (Busicom) to create a chip for a calculator
- It is the first microprocessor, i.e. the first processor-on-a-chip

Altair

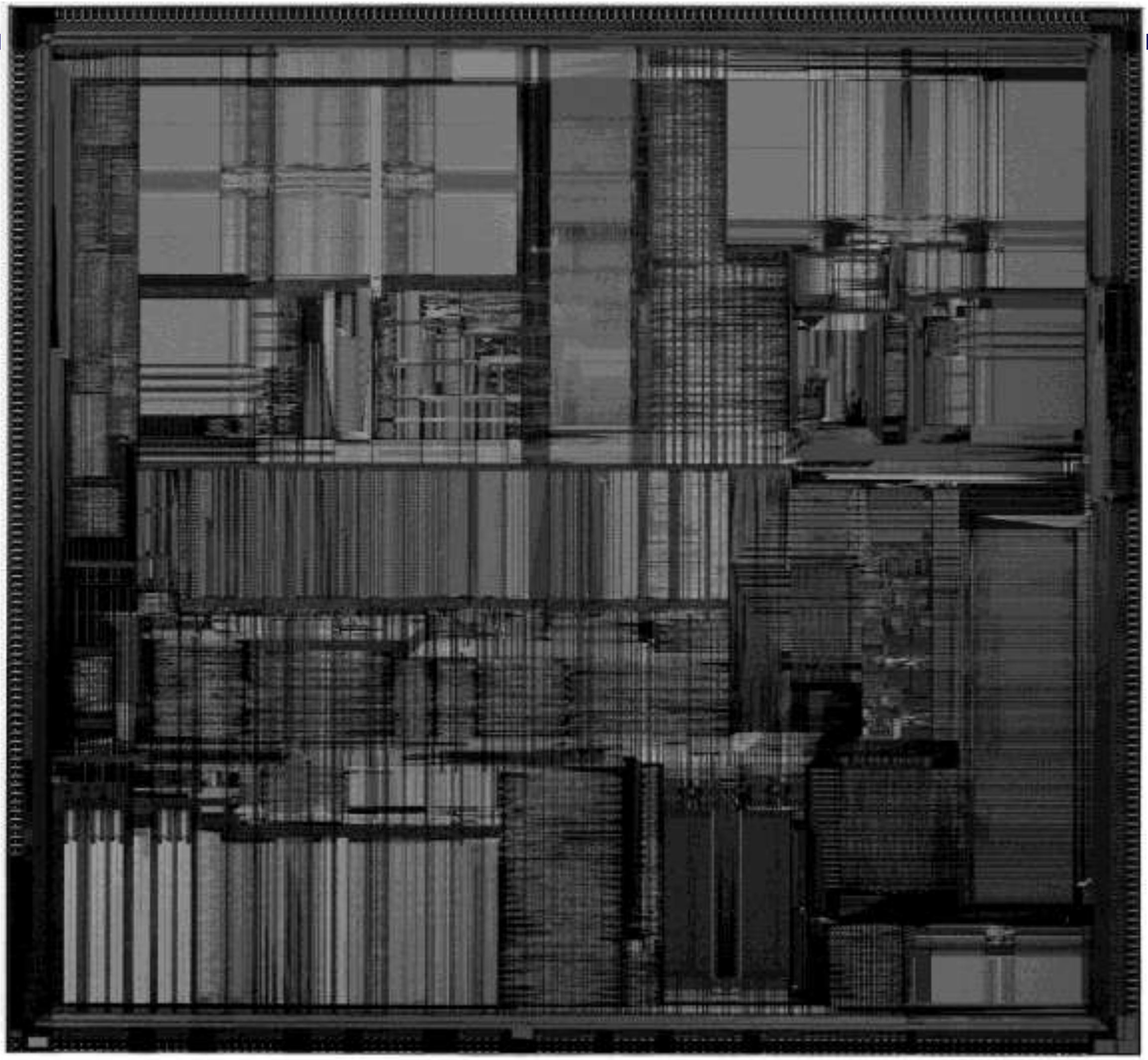


- Developers Edward Roberts, William Yates and Jim Bybee spent 1973-1974 to develop the MITS Altair 8800, the first personal computer.
- Priced $375, it contained 256 bytes of memory, but had no keyboard, no display, and no auxiliary storage device.
- Later, Bill Gates and Paul Allen wrote their first product for the Altair -- a BASIC compiler

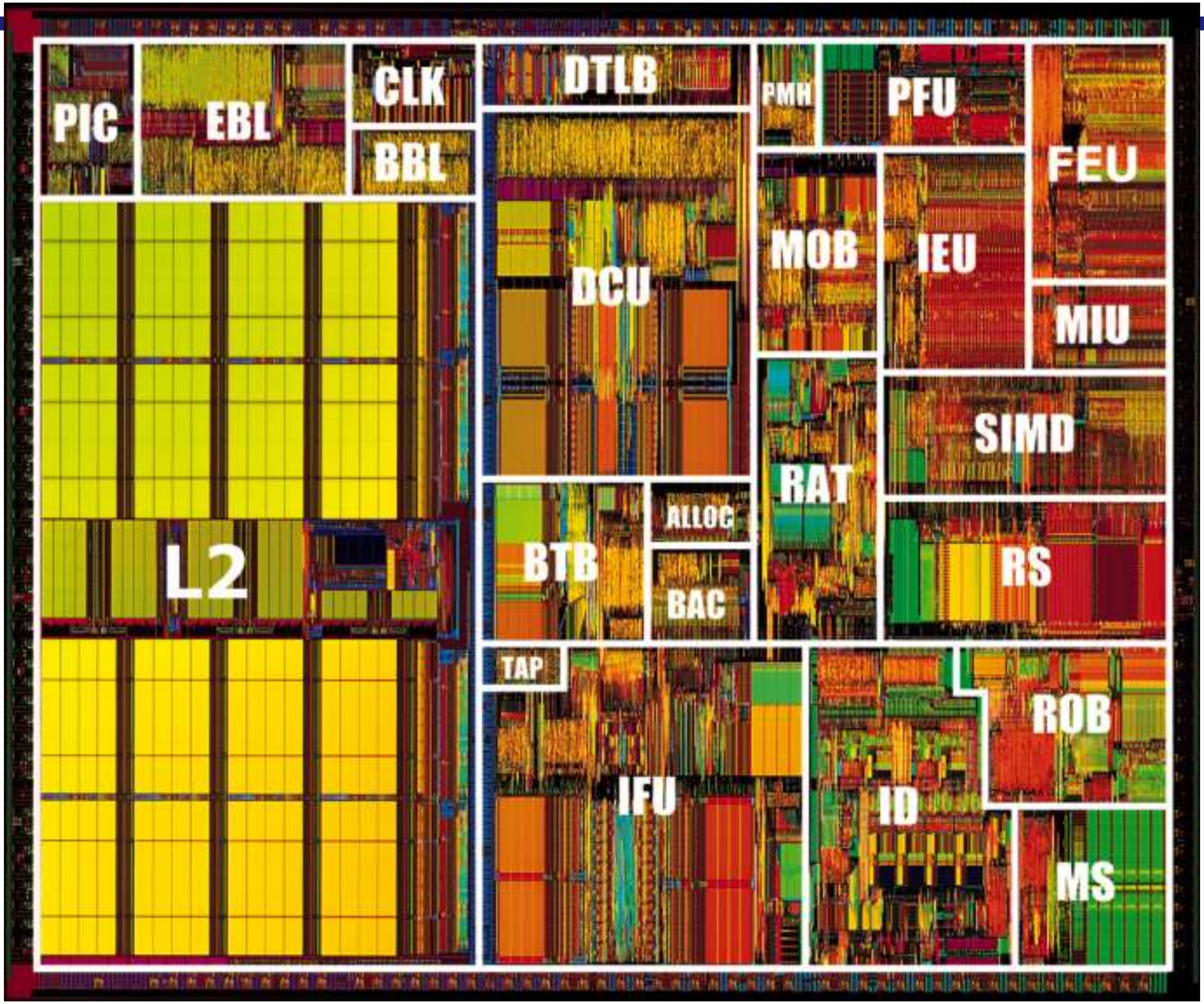
Intel 4004



Intel Pentium II



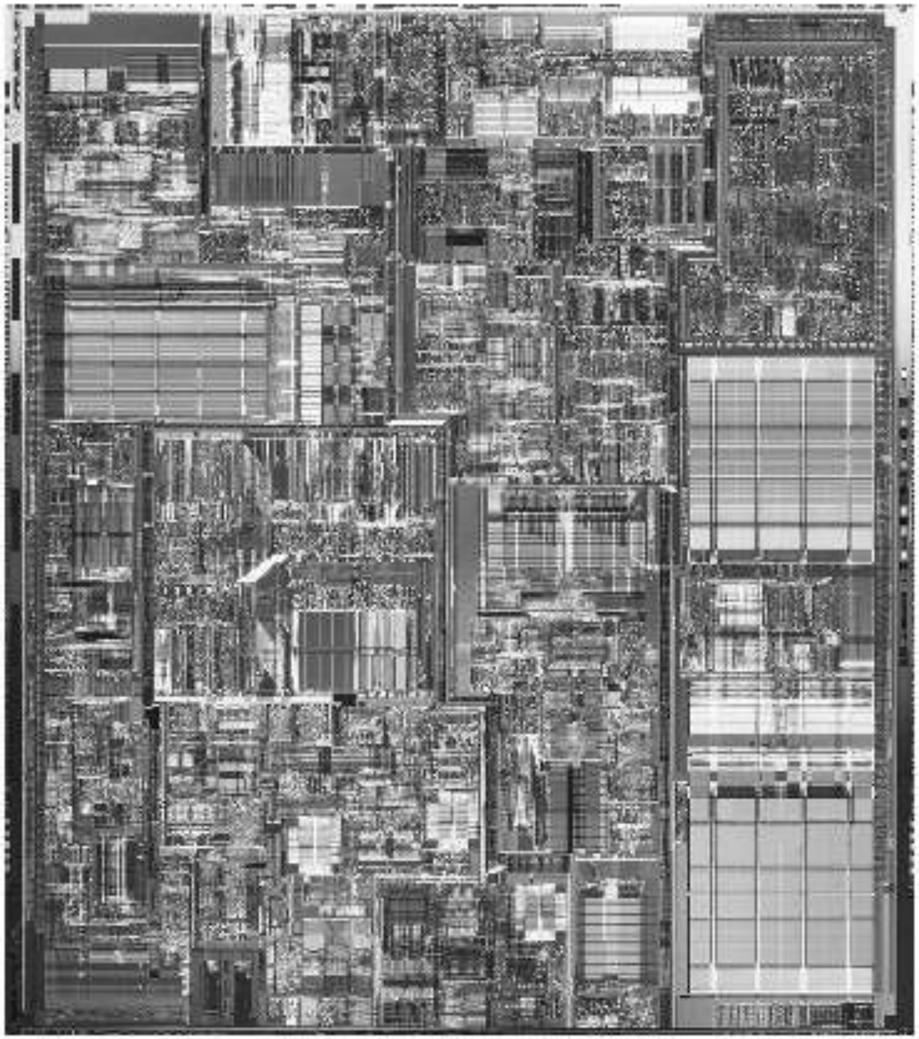
Pentium III (2000)



•**PIC**	**Programmable Interrupt Controller**
•**E/BBL**	**External/Back-side Bus Logic**
•**CLK**	**Clocking**
•**L2**	**Level 2 cache**
•**DTLB**	**Data Translation Look-aside Buffer**
•**DCU**	**Data Cache Unit**
•**BTB**	**Branch Target Buffer**
•**BAC**	**Branch Address Calculator**
•**TAP**	**Testability Access Port**
•**IFU**	**Instruction Fetch Unit**
•**PMH**	**Page Miss Handler**

- **PFU** **Packed FPU (MMX)**
- **SIMD** **Packed Floating point**
- **MOB** **Memory Order Buffer**
- **IEU** **Integer Execution Unit**
- **RAT** **Register Alias Table**
- **FEU** **FPU Execution Unit**
- **MIU** **Memory Interface Unit**
- **RS** **Reservation Station**
- **ID** **Instruction Decode**
- **ROB** **Re-Order Buffer**
- **MS** **Micro-instruction Sequencer**

Intel Pentium 4



Fall 2002

- 2.80 GHz
- 0.13-micron technology
- 478-pin package
- 512 KB L2 Cache
- 50 Amps
- Vcc = 1.5V

SONY PlayStation 2000

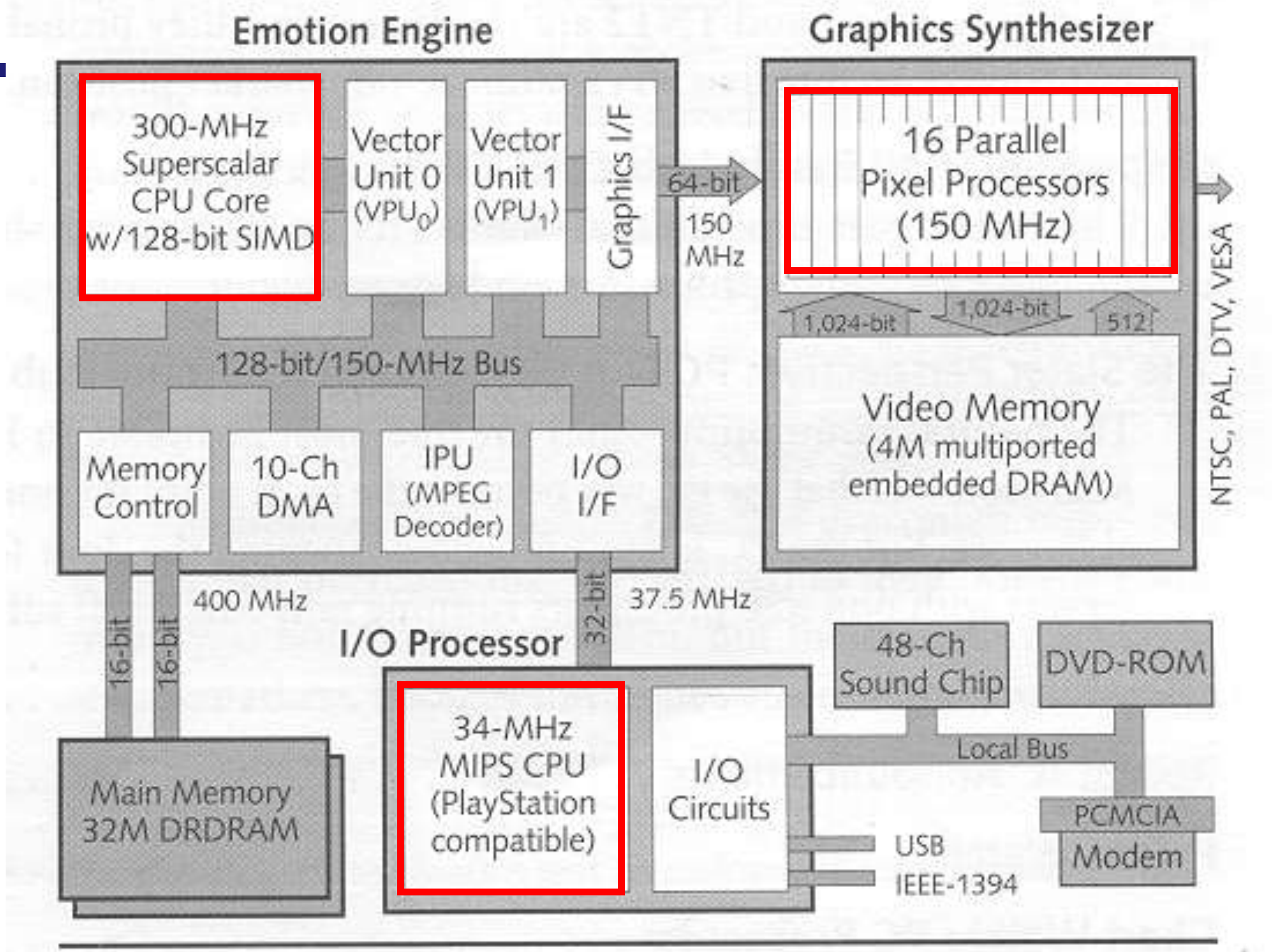
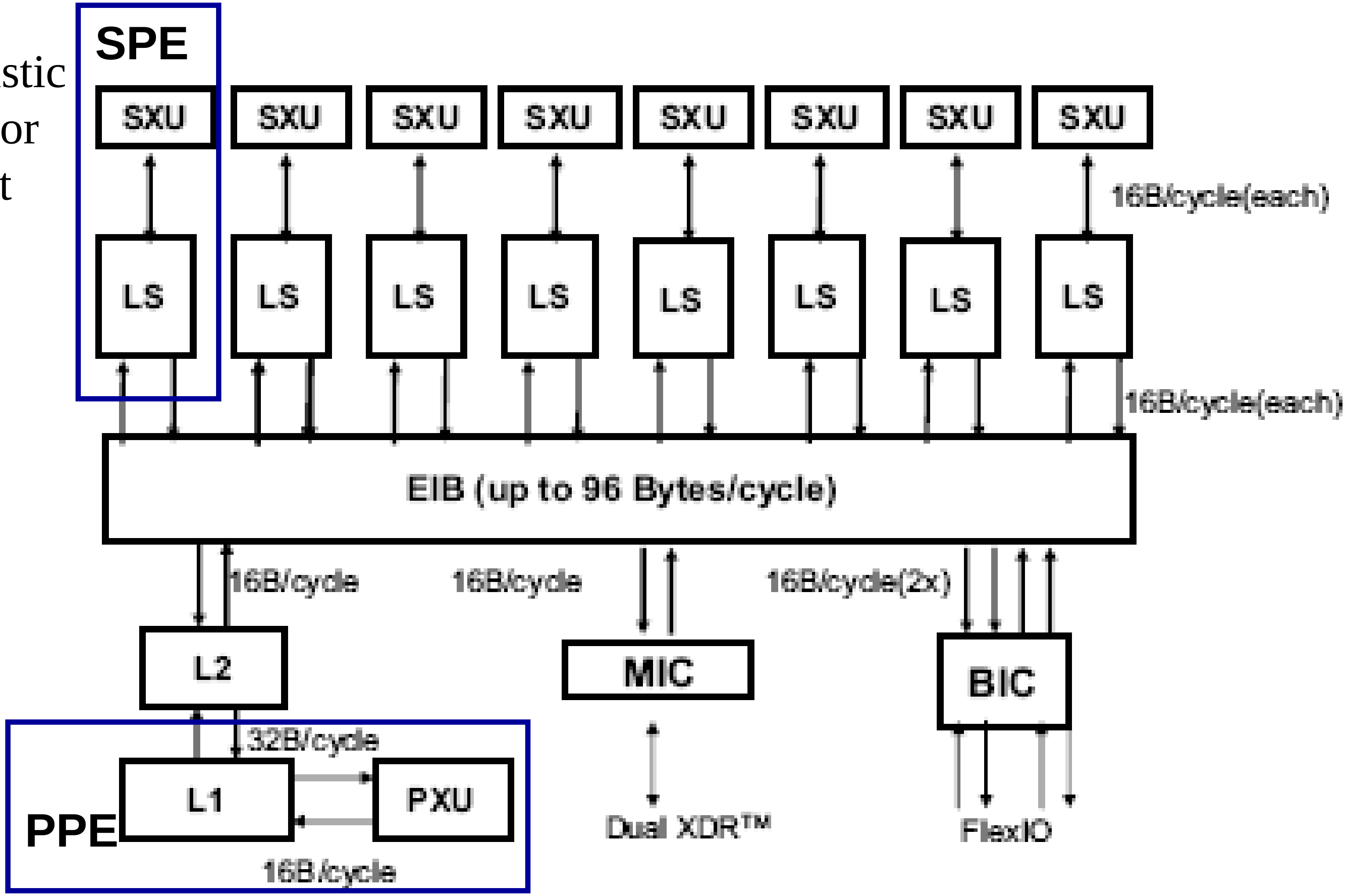


Figure 1. PlayStation 2000 employs an unprecedented level of parallelism to achieve workstation-class 3D performance.

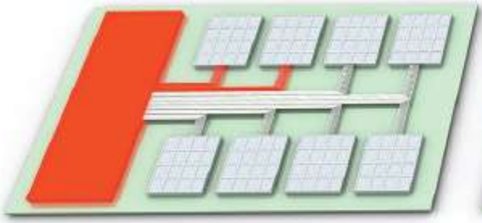
SONY PlayStation 3 Processor

Synergistic Processor Element

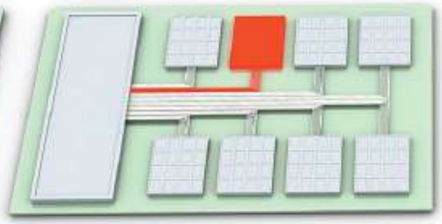


Power Processor Element

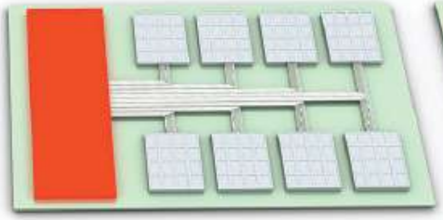
SPIKED: Two different types of processors share the work of the game in ***Resistance: Fall of Man***. When a player hurls a spike-flinging grenade at a monster, the Power Processor Element (PPE) asks two Synergistic Processor Elements (SPEs) to calculate collisions between the spikes and everything else. If a spike hits a monster, the PPE coordinates the work of other SPEs to determine the result of the impact.



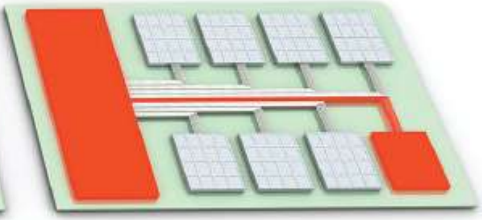
The PPE asks two SPEs if any of the spikes have collided with anything.



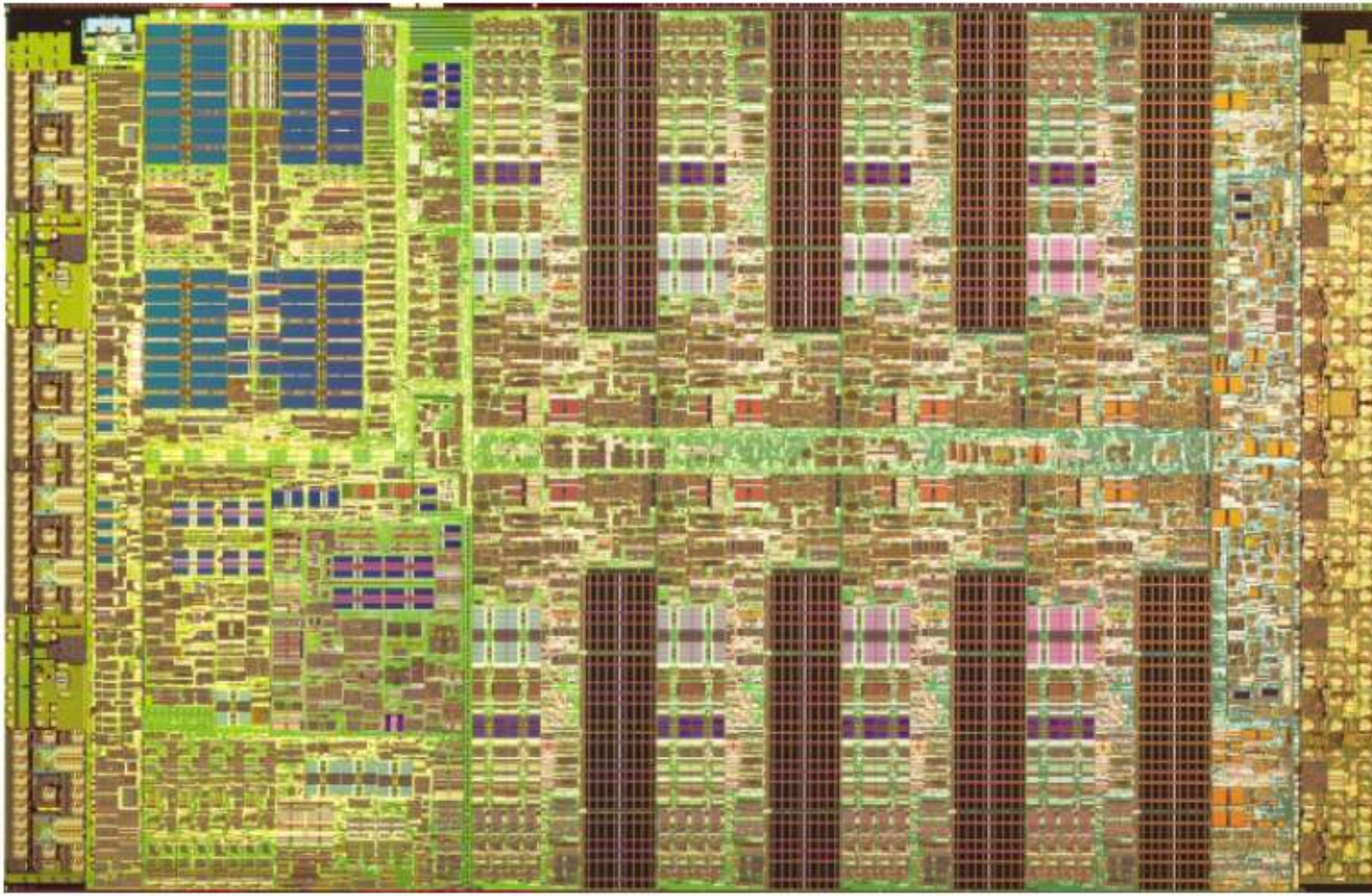
One SPE responds that a spike hit a Chimera in the gut.



The PPE determines that the spike has killed the Chimera.

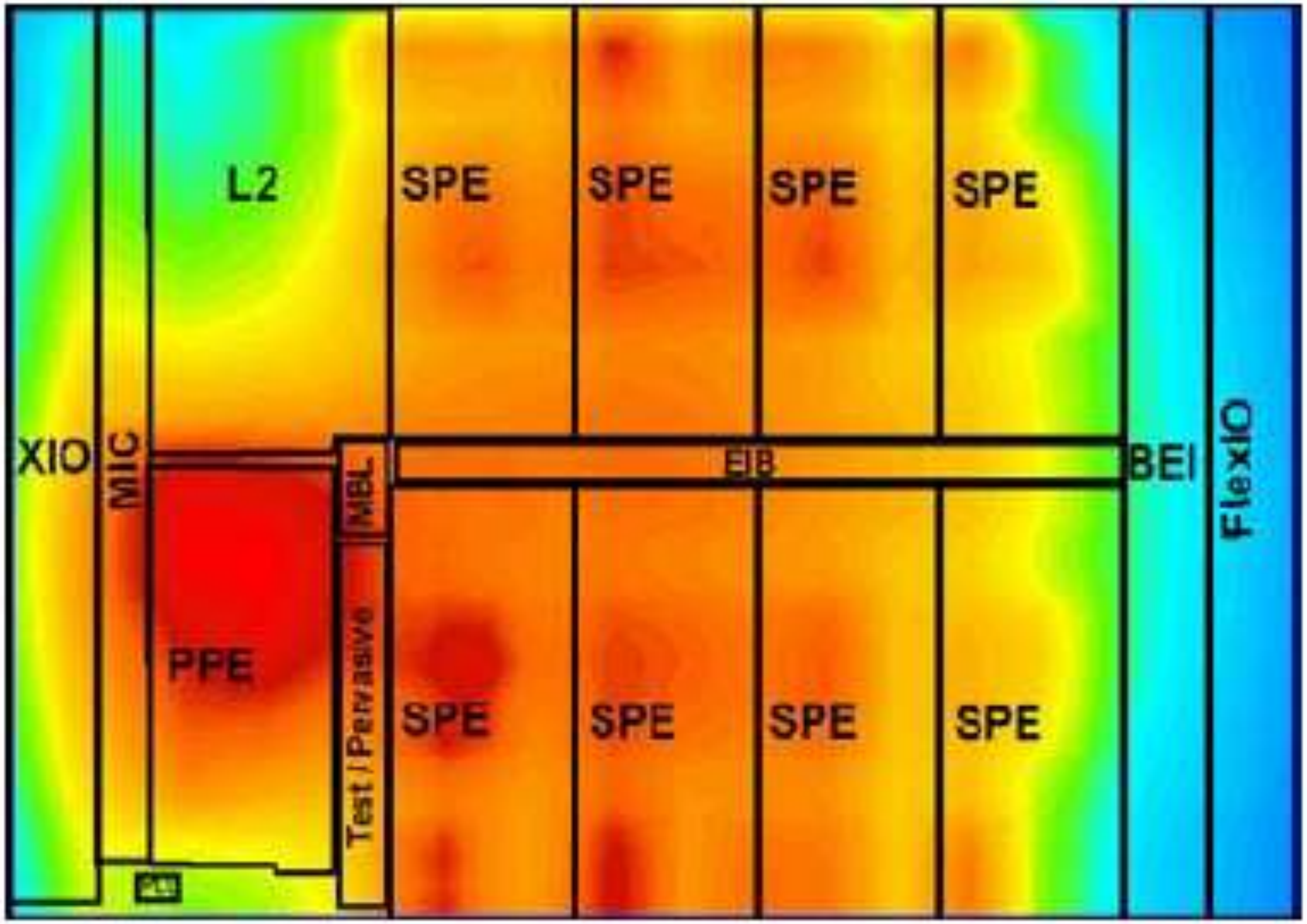


The PPE orders an SPE to compute the Chimera's physical response to the spike's impact.

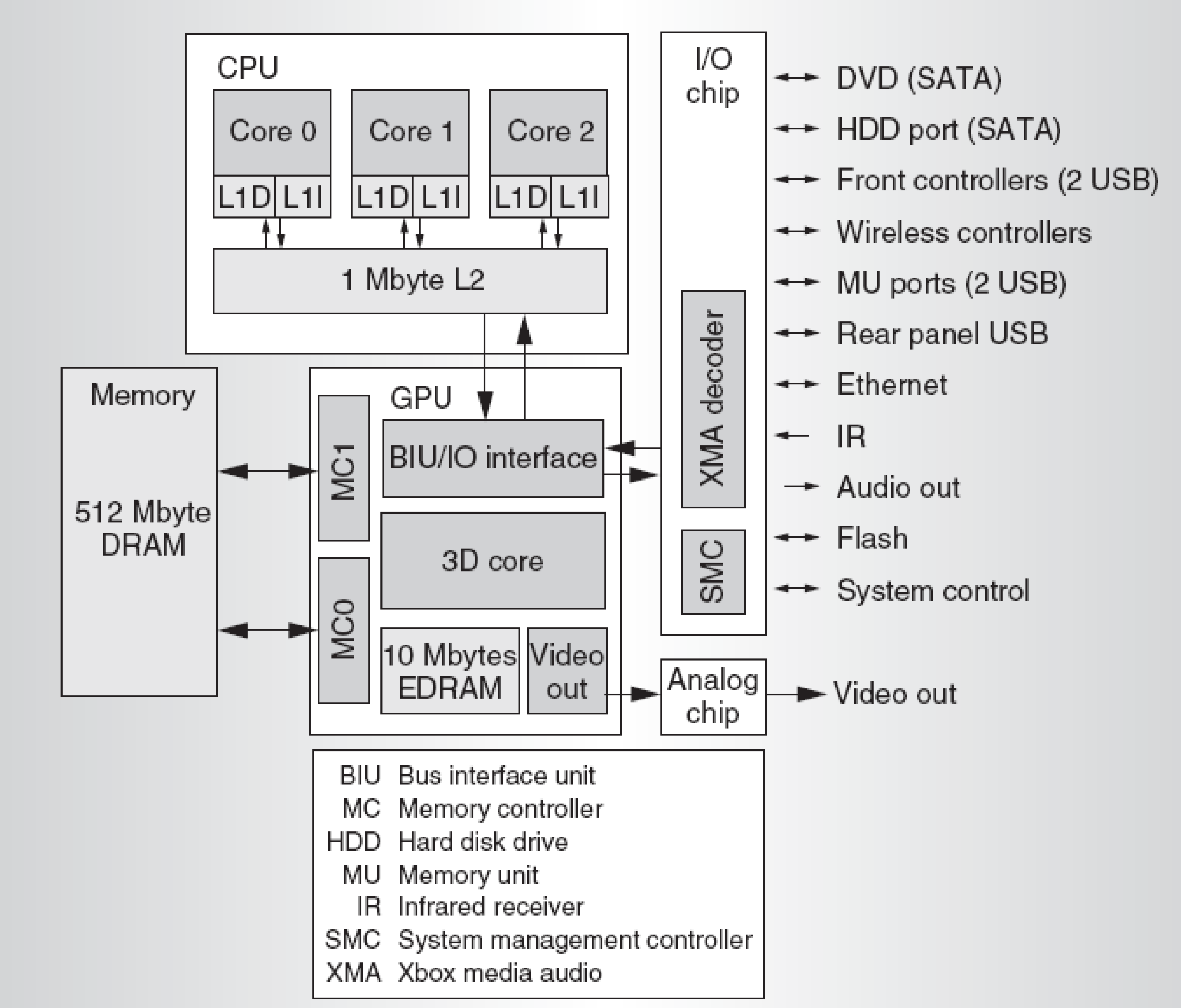


CELL CITY MAP: The Cell microprocessor that will power Sony's PlayStation 3 game console has nine processor cores. The core making up the left quarter of the chip is similar to the processors in Apple computers. The other eight cores, notable by their columns of memory [brown], are designed to do multimedia tasks.

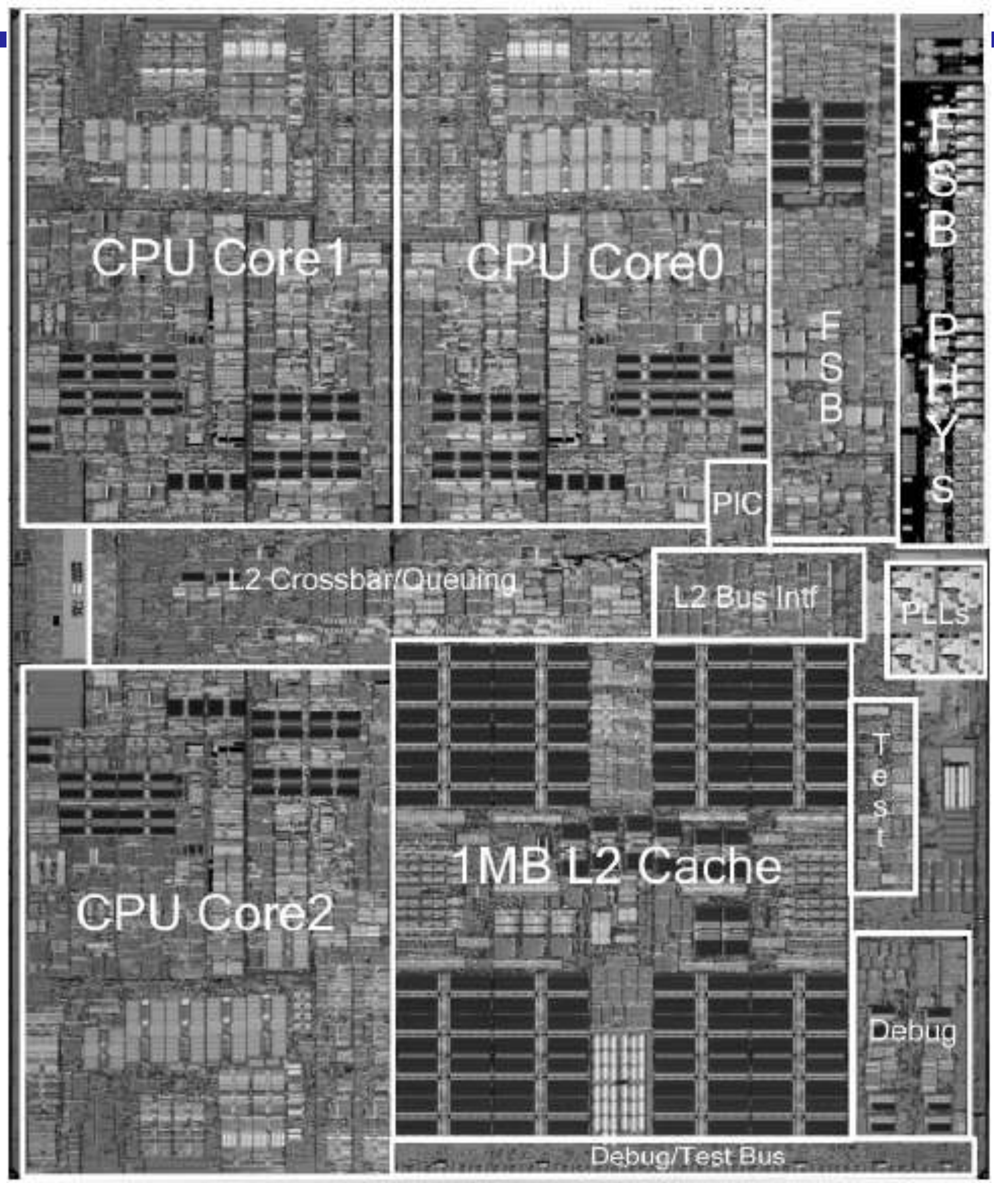
Chip Thermal Map



XBOX 360


CPU
Core 0
Core 1
Core 2
L1D
L1I
L1D
L1I
L1D
L1I
1 Mbyte L2
I/O
chip
XMA decoder
SMC
DVD (SATA)
HDD port (SATA)
Front controllers (2 USB)
Wireless controllers
MU ports (2 USB)
Rear panel USB
Ethernet
IR
Audio out
Flash
System control
Memory
512 Mbyte
DRAM
GPU
MC1
MC0
BIU/IO interface
3D core
10 Mbytes
EDRAM
Video
out
Analog
chip
Video out
BIU Bus interface unit
MC Memory controller
HDD Hard disk drive
MU Memory unit
IR Infrared receiver
SMC System management controller
XMA Xbox media audio

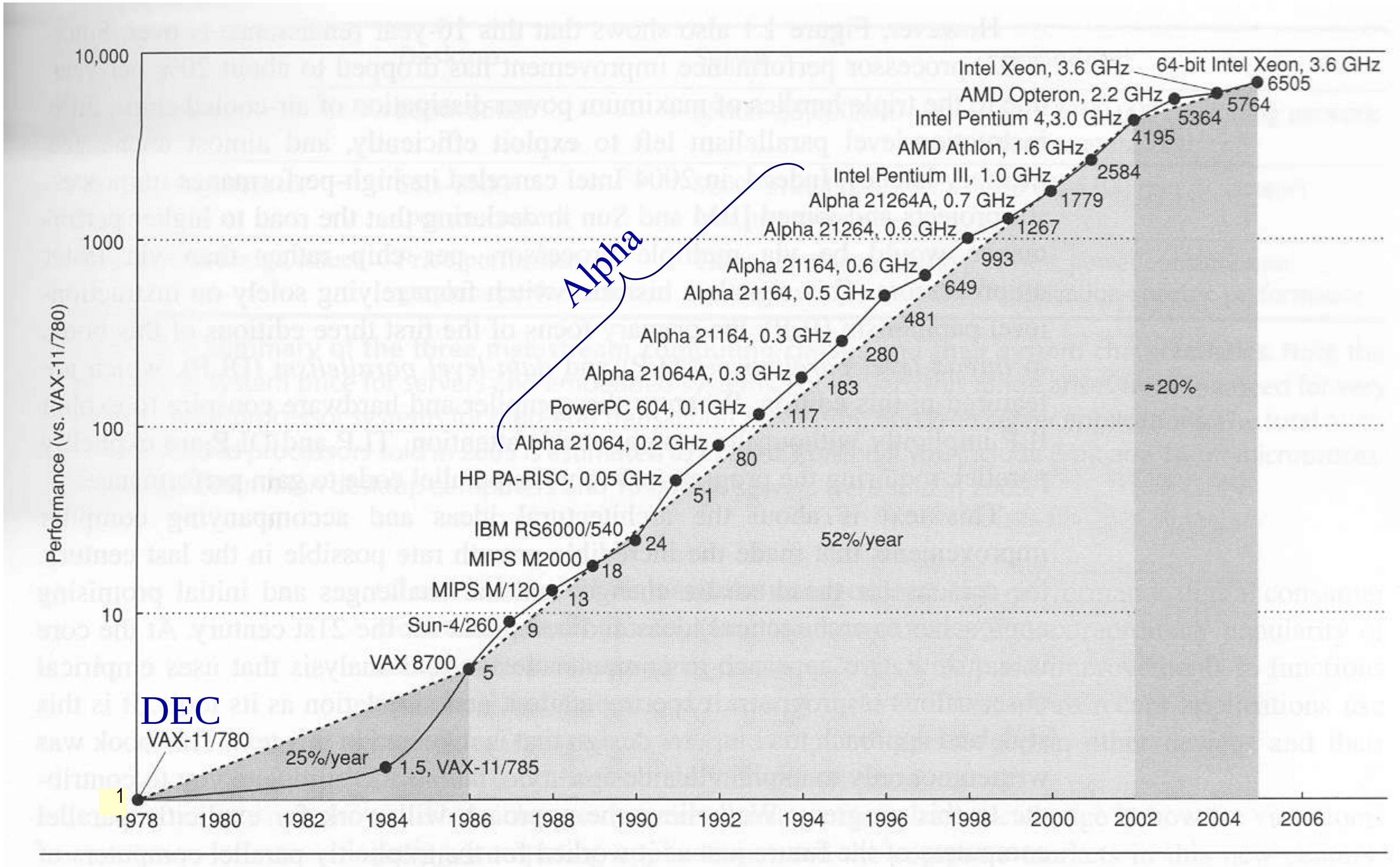
CPU (Xbox 360)


CPU Core1
CPU Core0
FSB
FSB PHYS
PIC
L2 Crossbar/Queuing
L2 Bus Intf
PLLs
Test
1MB L2 Cache
CPU Core2
Debug
Debug/Test Bus

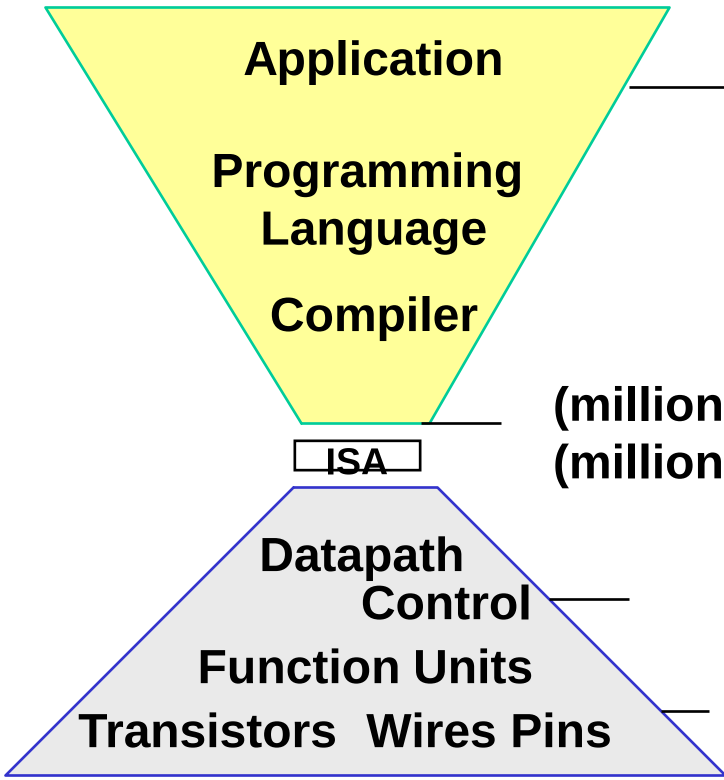
Why Such Change in 12 years?

- Performance
  - Technology Advances
    - CMOS VLSI dominates older technologies (TTL, ECL) in cost *AND* performance
  - Computer architecture advances improves low-end
    - RISC, superscalar, RAID, …
- Price: Lower costs due to …
  - Simpler development
    - CMOS VLSI: smaller systems, fewer components
  - Higher volumes
    - CMOS VLSI: same dev. cost 10,000 vs. 10,000,000 units
  - Lower margins by class of computer, due to fewer services
- Function
  - Rise of networking/local interconnection technology

Performance



Metrics of Performance



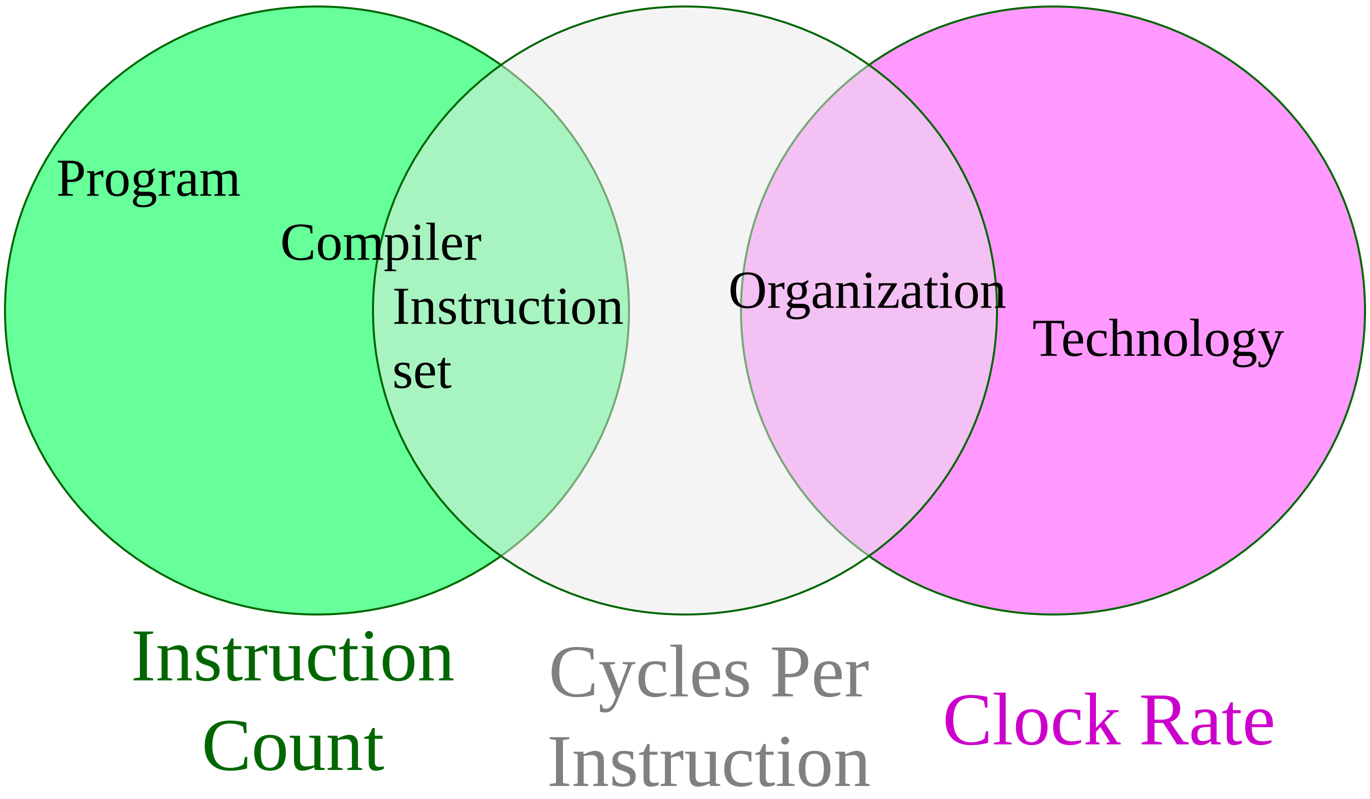
Answers per month
Operations per second

(millions) of Instructions per second: MIPS
(millions) of (FP) operations per second: MFLOP/s

Megabytes per second

Cycles per second (clock rate)

CPU time


Program
Compiler
Instruction
set
Organization
Technology
Instruction
Count
Cycles Per
Instruction
Clock Rate

Computer Architecture

Computer Architecture =

Instruction Set Architecture +

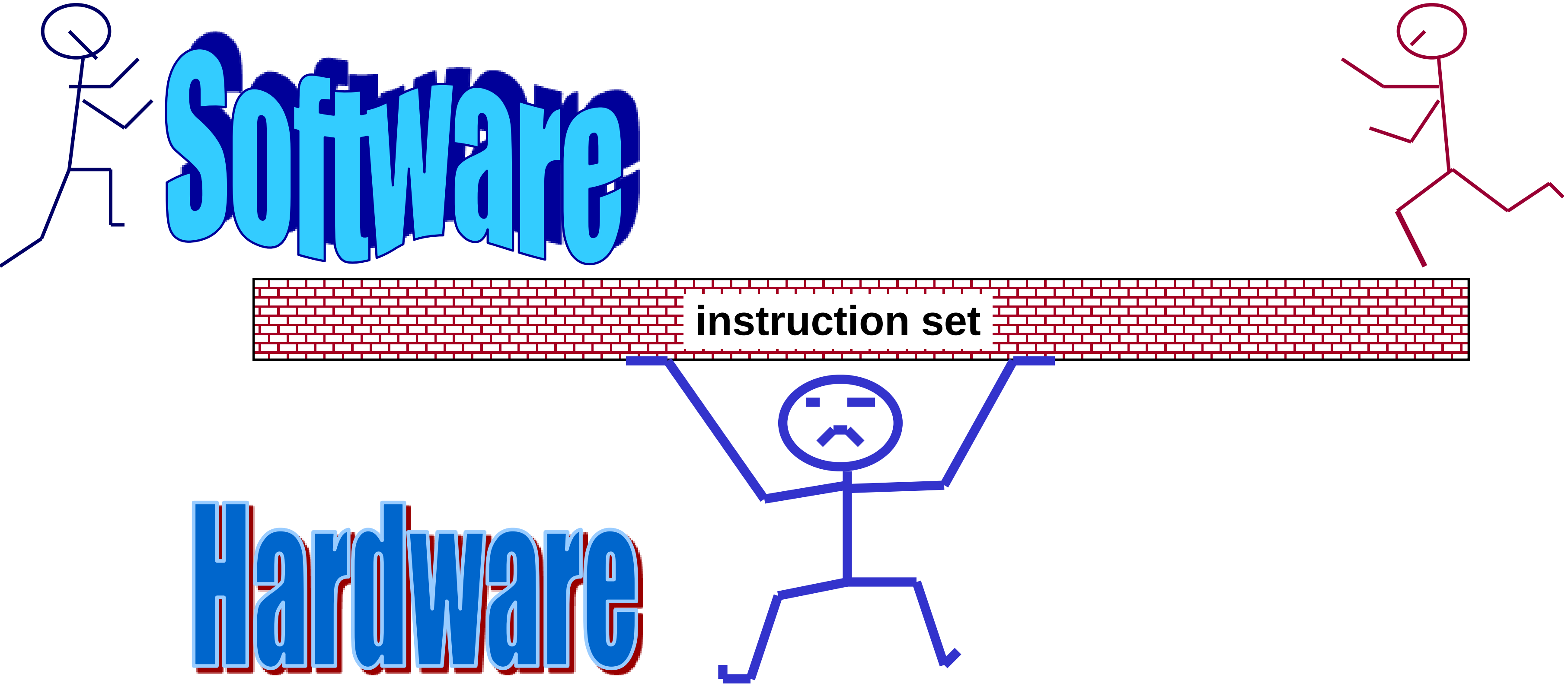
Machine Organization + …

Computer Architecture's Changing Definition

- 1950s to 1960s: Computer Architecture Course Computer Arithmetic
- 1970s to mid 1980s: Computer Architecture Course Instruction Set Design, especially ISA appropriate for compilers
- 1990s: Computer Architecture Course Design of CPU, memory system, I/O system, Multiprocessors
- 2000s: Computer Architecture Course

  Design of CPU (Performance & Power), Memory system, I/O, embedded systems, wireless.

Instruction Set Architecture (ISA)



Interface Design (ISA)

A good interface:

- **Lasts through many implementations (portability, compatibility)**
- **Is used in many different ways (generality)**
- **Provides convenient functionality to higher levels**
- **Permits an efficient implementation at lower levels**