EE 334 COMPUTER ARCHITECTURE Spring 2008

Sloan 233 M,W,F 9:10-10AM

Objectives: To provide a sound background in computer architecture. The main focus is processor design and evaluation with case studies. A number of architectural alternatives are described and evaluated using quantitative approaches. Pre-requisite: EE234

1. Computer Abstractions and Technology ***(Chapter 1)***

1.1 Programs
1.2 Integrated circuits
1.3 Microprocessors

2. Instruction Set Architecture ***(Chapter 2)***

2.1 Instruction types: Arithmetic, Logic, Branch, Memory
2.2 Operand storage, type and size
2.3 Examples of instruction sets (MIPS)

3. Computer Arithmetic ***(Chapter 3)***

3.1 Number representation
3.2 Addition/subtraction
3.3 ALU
3.4 Multiplication/division
3.5 Floating point

4. Processor Architecture ***(Chapter 4)***

4.1 Building a datapath
4.2 Pipelining principle
4.3 Pipelined datapth and control
4.4 Data hazards and forwarding
4.5 Control (branch) hazards
4.6 Instruction-level parallelism
4.7 AMD Opteron X4

5. Memory Hierarchy ***(Chapter 5)***

5.1 Principle of locality
5.2 Memory hierarchy
5.3 Cache memory
5.4 Virtual Memory

6. Multicore and Multiprocessor ***(Chapter 7)***

6.1 Parallel Processing
6.2 Share Memory Multiprocessors
6.3 Hardware Multithreading
6.4 Message passing multiprocessors

Textbook: D. A. Patterson and J. L. Hennessy, *Computer Organization and Design: The Hardware/Software Interface,* **Fourth Edition**. Morgan Kaufmann Publishers, 2009.

Grade:	2 Exams (30% each)	60%
	Homework	20%
	Final Exam	20%

Instructor: Dr. José Delgado-Frias Office: EME 502
Email: jdelgado@eecs.wsu.edu Phone: (509)335-1156 Fax: (509)335-3818

Office Hours: Wednesday 10:30am – 12noon (or by appointment.)