EE334 ***Name:*** \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_

Computer Architecture Homework Assignment 7 March 28, 2011 (9:10AM)

Clara, a senior engineer, at C3 (Creative Computer Corporation) is working on a new pipelined processor. She has a benchmark that has the following characteristics:

33% ALU instructions,

27% load instructions

 (15% of loads are followed by instructions that use the data being loaded)

16% store instructions

24% branch instructions (58% of these branches are taken).

This processor’s CPIint is 1 (when there are no hazards). Please answer the following questions:

1. Considering control and data hazards, please compute the overall CPI. Assume that all branch instructions cause hazards (the penalty is 1 clock cycle; actually, a NO-OP instruction is inserted after every branch).
2. Some instructions (in order to remove some NO-OPs) can be moved to the delay slot without causing any side effects on the program execution. Remember, the instruction after the branch is always executed by this machine. Some of the NO-OPs are replaced as follows: 11% with an instruction from the before the branch and 9% with an instruction from the target. Please compute the new CPI.
3. Clara has incorporated a branch target buffer (BTB) into this machine. The BTB performs as follows: 91% of the branches are found in the BTB, 93% of the braches in the BTB are correctly predicted. When a branch is mispredicted or is not found and taken the processor cancels the instruction that has been fetched. Please determine the new CPI.