Reducing Power and Delay in Memory Cells Using Virtual Source Transistors

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***Abstract*—Seven novel static RAM cells are described in this paper. All seven are a variation of the six-transistor differential memory cell containing a two-inverter feedback loop with n-type pass transistors between the inverter inputs and the bit-lines. Each variation contains some combination of virtual source transistors (Virtual Ground or V_{DD}) and transmission gates. Power and delay values are given for each of the seven designs with minimum sized transistors, as well as a discussion of improved performance with wider pass transistors. The new cells with the best performance in the areas of power consumption, delay, and power-delay product demonstrate improvements of 27.6%, 12.2%, and 24.1% respectively.**

I. Introduction

Memory cells are used in a number of applications in digital systems. These applications range from memory arrays to reconfigurable systems such as FPGAs. SRAM (static random access memory) cells are of particular importance in high-performance digital systems, since these cells need no refresh and are much faster than the dynamic ones.

The basic SRAM cell (called in this study: $Basic_N$ cell) is shown in Figure 1 [1,2,3]. As can be seen in the figure, several short circuits exist when a write operation is performed. The first is between the V_{DD} and Gnd sources to the inverter loop's transistors. The second is from V_{DD} to the bit-line at Logic 0. There is also a short circuit between the bit-line at Logic 1 and Gnd. All three of these short circuits only exist when a memory cell is switching its stored value; however, they do lead to significant power consumption and therefore are a problem. Another problem with the $Basic_N$ cell is its delay. The speed at which a memory cell can be written to and read from is very important since these are common tasks. Also, longer switching times mean greater power consumption, especially when short circuits exist. The work discussed in this paper seeks to decrease both delay and power consumption through the design of seven novel SRAM cells

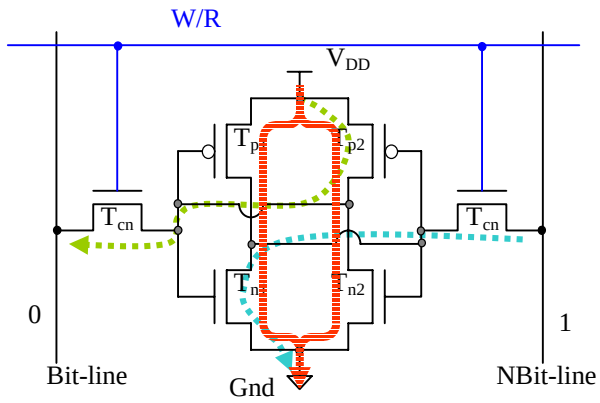

Figure 1. Basic Cell

The organization of this paper is as follows. First the three major modifications made to the $Basic_N$ cell are discussed in Section II. Then, in Section III, a discussion of the scheme for the timing of the write signal along with the ON and OFF time of the virtual source transistors follows. Section IV describes the seven novel SRAM cell designs. Techniques used in this study for measuring power and delay as well as the performance evaluations of each cell are covered in Section V. And Section VI concludes with a final discussion of the memory cells with the best performance.

II. Cell Modifications

As described earlier, there are some inherent problems with the $Basic_N$ memory cell. In this section three additions to the $Basic_N$ cell are presented, each designed to eliminate one of those problems. The proposed modifications have some similarities with differential memories [4].

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A. *Virtual Ground*

One of the biggest sources of power loss in the $Basic_N$ memory cell is the short circuit that briefly exists between V_{DD} and Gnd when a write cycle that causes the cell's value to switch is being executed (a *switching* write cycle). For a brief period of time both the n- and p-type transistors of each inverter are ON. To remove this problem, a n-type transistor is placed between Gnd and the inverter's nMOS transistors. This is shown in Figure 2, as the transistor labeled T_{VG}. The name Virtual Ground comes from the transistor's location in the memory cell. The transistor is seen by the inverters as the source for Gnd, hence it is a Virtual Ground.

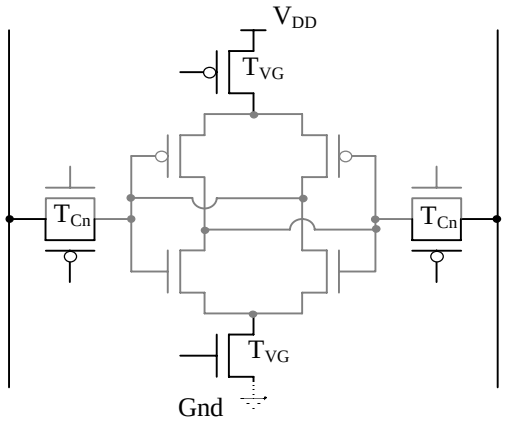

Figure 2. Modifications to the Basic Cell.

B. *Virtual V_{DD}*

The short circuit that exists momentarily between V_{DD} and the Logic 0 bit-line is a second source of power loss in the $Basic_N$ memory cell. This path exists only during switching, although in this case it is through the pMOS transistor of one inverter and to the opposite bit-line (the one switching to 0) attached to the inverter's feedback loop. The path described is shown as the top dotted line in the schematic of Figure 1. Finally, as explained for the Virtual Ground transistor, this new transistor is named for the fact that it is a Virtual source of V_{DD}. It is shown as the transistor labeled T_{VV} in Figure 2.

C. *CMOS Transmission Gates*

Delay is another area of concern for SRAM cells. By placing a pMOS pass transistor in parallel with the nMOS pass transistors (each labeled as T_{Cn} in Figure 1), two problems with the $Basic_N$ cell are removed. First, the transmission gate allows for both a strong Logic 1 and a strong Logic 0 to pass to the inverter loop of the $Basic_N$ memory cell, which shortens the delay by allowing the cell to switch faster. Second, the presence of a strong Logic 1 at one of the inverter inputs helps to further prevent the short circuit from V_{DD} to the Logic 0 bit-line by causing the p-type transistor to switch faster. In Figure 2, the additional p-type transistors are labeled as T_{Cp}. The combination of each T_{Cp} and T_{Cn} make up a CMOS transmission gate and from now on will be referred to as T_C.

III. VIRTUAL TRANSISTOR TIMING SCHEME

In order for both the T_{VG} and T_{VV} transistors to be of any use once implemented in a memory cell, the timing for turning each ON or OFF must be very precise. Figure 3 shows the basic timing scheme for writing to a memory cell containing T_{VG} (for T_{VV}, the $NotW_\Delta$ signal voltage would be inverted). The timing diagram demonstrates how T_{VG} must be turned OFF just before writing, but then turned back ON before the write cycle has completed to ensure that the feedback inverters (InvL and InvR) have a strong voltage sourcing their inputs. This promotes both the minimum delay of the cell as well as ensuring that a short circuit does not occur. WE signal (write enable) is used to generate the proper Writer signal (W/R) and $NotW_\Delta$.

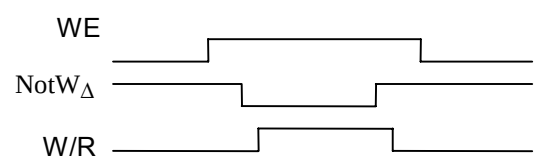

Figure 3. Timing requirements for a write operation.

IV. SRAM CELL DESCRIPTIONS

In Section II, three innovative modifications to the $Basic_N$ SRAM cell were described. Each of these, alone or in combination with the others, leads to a different form of the $Basic_N$ cell. Table 1 shows the configuration for each new memory cell as well as its full name and abbreviation. Each memory cell is named according to the modifications made to it. For example, the first cell to be discussed is VG_N, named for the fact that it contains a Virtual Ground transistor and still uses the nMOS pass transistors instead of the transmission gates. A description of the seven novel SRAM cells follows.

Table 1. Memory cell configurations.

Memory Cell Name		**T_{VG}**	**T_{VV}**	**T_C**
nMOS Virtual Ground	VG_N	X		
nMOS Virtual V_{DD}	VV_N		X	
nMOS Virtual Ground/V_{DD}	VGV_N	X	X	
CMOS Basic	$Basic_C$			X
CMOS Virtual Ground	VG_C	X		X
CMOS Virtual V_{DD}	VV_C		X	X
CMOS Virtual Ground/V_{DD}	VGV_C	X	X	X

Each of these modifications is explained below.

nMOS Virtual Ground (VG_N). The VG_N memory cell has the same overall structure as the $Basic_N$ cell, except that it also contains a nMOS transistor between Gnd in the cell and the n-type transistors of the inverters in the memory. It is designed specifically to remove the temporary path from V_{DD} to Gnd and by doing so, to save power.

nMOS Virtual V_{DD} (VV_N). This cell contains a Virtual V_{DD} transistor, but otherwise is the same as the $Basic_N$ memory. The intent of this design is to remove the direct path from V_{DD} to the Logic 0 bit-line and reduce power consumption.

nMOS Virtual Ground/V_{DD} (VGV_N). This memory cell design handles both forms of the short circuit path between V_{DD} and either Gnd in the cell or on the bit-line. It is built like the VG_N cell with the addition of the Virtual V_{DD} transistor between the p-type transistors of the memory's feedback loop and the V_{DD} source.

CMOS Basic ($Basic_C$). The $Basic_C$ SRAM simply replaces the nMOS pass transistors of the $Basic_N$ memory with transmission gates that supply strong logic values to the feedback loop of the cell. As explained in section 2, the goal of this design is to generate faster write times and also to control the effects of the brief short circuit between V_{DD} and the Logic 0 bit-line.

CMOS Virtual Ground (VG_C). The combination of having both the CMOS transmission gates and the T_{VG} transistor is supposed to shorten the time to switch the value of the memory cell and to delete the short circuit power between V_{DD} and Gnd.

CMOS Virtual V_{DD} (VVc). This cell essentially is the VV_N SRAM with CMOS transmission gates; it is intenended to improve on the delay of the VV_N cell and to have a lower power consumption than the $Basic_N$ cell.

CMOS Virtual Ground/V_{DD} (VGV_C). The VGV_C memory focuses on the problem of delay in the VGV_N cell. By including the T_C transistors, switching can occur at an increased rate. The presence of both the T_{VG} and T_{VV} transistors allows for a reduction in the power wasted in the $Basic_C$ cell.

V. Performance Measurement and Evaluation

This section begins by describing several methods for accurately measuring the power and delay of each SRAM. After that, a comprehensive discussion and analysis regarding the performance of each cell is given.

A. Techniques for Measuring Power and Delay

To best simulate a memory cell as it would function in a full 32X32 bit memory, the cell to be measured is given input logic that creates the delays and capacitances that can be expected. For measuring the power during a write cycle to this cell, two different voltage sources are created: one for the hardware external to the memory cell (such as the input logic) and one for the memory cell itself. This allows for power to be monitored for the memory cell alone and therefore compared more accurately with other cells. The power is measured as the total power used during one write cycle, and as long as the timings for write cycles are uniform over the different memories, this is a safe method for comparing power consumption of each cell.

The other measurement to be recorded is that of delay. In order to measure the time it takes to write to a cell, the time at the 50% voltage mark for a switching pass transistor is recorded followed by the time of the 50% mark for the inverters in the memory. The longer of the delays for the two inverters (the rising inverter is always slower with minimum sized transistors) is the value then used for comparison with other memory cells. Figure 4 is a simulation (using the Cadence SPICE simulator) of the VG_C memory cell based off of the timing scheme described in section 3. In this simulation, delay would be measured between the rising sides of both the W/R and the InvR signals.

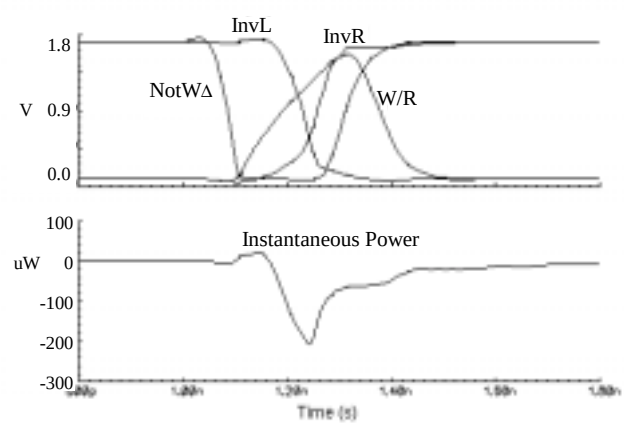

Figure 4. Simulation of a VG_C memory cell.

B. Performance

The data in Table 2 shows the measurements for power, delay, and power-delay product for each of the different SRAM configurations. These values are for each of the memory cells with every transistor at minimum size. Once transistor sizes are changed, performance begins to vary. These variations will only be discussed for cells that are affected significantly.

The first two of the new designs, VG_N and VV_N, both reduce the power consumed considerably, although in comparison with $Basic_N$, the delay becomes worse for VV_N while it gets better for VG_N. Delays for both of these can be improved by increasing the widths of T_{Cn} (and T_{VV} in the case of VV_N) by two or three times, but power consumption will then also increase. The next design, VGV_N utilizes both T_{VV} and T_{VG}, and as expected, it demonstrates the lowest power consumption. Unfortunately, the delay is greater than the $Basic_N$ cell by 22.6%.

The next four SRAM designs make use of the T_C transistors. With the exception of the $Basic_C$ cell, all of these successfully reduce the delay of their n-type counterparts: VG_C decreases by 5.8% from VG_N, VV_C by 18.2% from VV_N, and VGV_C improves on VGV_N by 21.1%. VG_C gave the shortest delay overall, with a savings of 12.3% over the $Basic_N$ SRAM. Power consumption, while in general is less for each cell using T_C transistors than for $Basic_N$ cell, is not an improvement over the n-type memories. If delay reduction is seen as the main concern, the use of any of the T_C memories is effective—especially if the widths of the T_{Cn} transistors are increased. In the $Basic_C$ SRAM, increasing the width of T_{Cn} by four or five times leads to a delay that is about 18% less than that of the $Basic_N$ at minimum sizing and 9% at similar widths.

Table 2. Power, delay and power-delay product comparisons

Configuration	Power (fJ)	Delay (ps)	Product
$Basic_N$	27.75	83.24	2309.91
VG_N	22.66	77.42	1754.33
VV_N	22.19	103.00	2285.57
VGV_N	20.09	101.51	2039.33
$Basic_C$	31.28	83.98	2626.89
VG_C	24.72	72.96	1803.57
VV_C	25.06	84.30	2112.55
VGV_C	22.40	80.07	1793.56

Figure 5 gives a more visual comparison between the cells and their power and delay values. This figure shows the potential tradeoffs that designer may face. It should be pointed out that all the new configurations (except for the $Basic_C$ cell at minimum sizing) show better power savings than the basic cell.

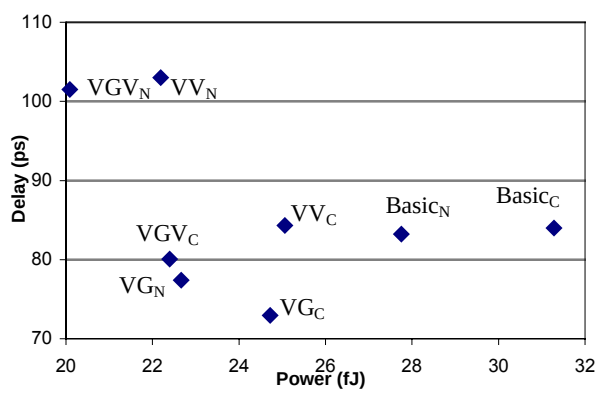

Figure 5. Plot of Delay and Power for Memory Cells.

VI. Concluding Remarks

In this paper, seven novel SRAM cells have been presented, their defining characteristics explained and their performance analyzed. Performance was measured in terms of power, delay, and the power-delay product. Following are the cells with the top performance in each category.

- *Lowest Power Consumption.* The VGV_N cell demonstrates the lowest power consumption during a write cycle and uses 27.6% less power than the $Basic_N$ memory cell. Including both T_{VG} and T_{VV} proved to be an effective way to reduce power consumed through short circuits.
- *Shortest Delay.* The SRAM cell that gives the shortest delay is the VG_C memory cell. Compared to the $Basic_N$ cell, VG_C has a delay that is 12.2% shorter. The combination of T_{VG} and the T_C transistors is valuable in the task of reducing delay in SRAM cells.
- *Smallest Power-Delay Product.* This is exhibited by the memory containing T_{VG} as its only addition. VG_N reduces delay by 7.0%, power consumption by 18.3%, and has a power-delay product of 24.1% less than the $Basic_N$ memory cell.

The results obtained in this study clearly indicate that there is a tradeoff between performance and power. The choice of a SRAM cell depends on the design constraints and required system capabilities. Architectural and application specific techniques can be used to further improve performance of the proposed cells.

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