Part III

Fault Ride Through and Post-Fault Recovery of Inverter Based Resources

Saeed Lotfifard
Ali Maleki, Graduate Student

Washington State University

For information about this project, contact

Saeed Lotfifard
Washington State University
School of Electrical Engineering and Computer Science
Pullman, Washington 99164-2752
Phone: 509-335-0903
Email: s.lotfifard@wsu.edu

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Power Systems Engineering Research Center
Arizona State University
527 Engineering Research Center
Tempe, Arizona 85287-5706
Phone: 480-965-1643
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NOMENCLATURE

IBR	Inverter base resources
FRT	Fault ride-through
PV	Photovoltaic
AW	Anti-windup
PBSMC	Proxy Based Sliding Mode Controller
SMC	Sliding Mode Controller
PLL	Phase-locked loop
DDSRF PLL	Decoupled double synchronous reference frame-PLL
Iref-q	Reference value of current in q frame
Iref-d	Reference value of current in d frame
v_{id}, i_d, v_{iq}, i_q	Current, and voltage of inverter, in dq0 reference frame.
C	Capacitor of the dc link
U	Modulation control signal determined by the MPPT algorithm
I_{max}	Maximum current of the inverter
$I_{nominal}$	Nominal current of the inverter
V_{max}	Maximum voltage of the inverter
$V_{di-no\ limit}$, $V_{qi-no\ limit}$	Voltage of inverter in d and q frame without considering V_{max} limit
$V_{di-modified}$ and $V_{qi-modified}$	Voltage of inverter in d and q frame considering V_{max} limit
$v_{d+}, v_{q+}, v_{d-}, v_{q-}$	Positive and negative sequence voltage at inverter terminal in dq frame
$i_d^+, i_q^+, i_d^-, i_q^-$	Positive and negative sequence current flows in the inverter in dq frame.
$i_{ref-d}^+, i_{ref-q}^+, i_{ref-d}^-, i_{ref-q}^-$	Positive and negative sequence reference current in dq reference frame
k_p, k_i and k_d	Proportional, integral and derivative gains of PID controller
x and x_p	Position of controlled object and position of the proxy
x_d	Desired position of the controlled object
λ	Gain of SMC
m	Mass of the proxy
f_{smc}, f_{PID}	Force produced by SMC, PID
S_{PBSMC}	Sliding surface of PBSMC

ω	Angular velocity
φ_a^+, φ_a^-	Phase angle of positive and negative sequence
$v_{d+}^*, v_{d-}^*, v_{q+}^*, v_{q-}^*$	Positive and negative sequence voltage at the inverter terminal in dq reference frame.
$i_{d+}^*, i_{d-}^*, i_{q+}^*, i_{q-}^*$	Reference value of positive and negative sequence current flow in the inverter in dq reference frame.
P_0, Q_0	Average values of the instantaneous active and reactive powers respectively
P_c, P_s, Q_c, Q_s	Oscillatory terms of instantaneous power in unbalanced situation
P_{ref}, Q_{ref}	Reference values for the active and reactive power

1. Fault Ride Through and Post-Fault Recovery of Inverter Based Resources

1.1 Background

In modern power grids, the integration and deployment of inverter base resources (IBRs) increase. Ensuring the fault ride-through (FRT) capability of grid-connected IBRs is of special importance. Upon occurrence of faults, IBRs should remain connected to the grid and support the grid by injecting reactive currents. Moreover, once the fault is cleared, IBRs should seamlessly transition into the post-fault condition. One of the main challenges in realizing this feature for IBRs is addressing the saturation of controllers of IBRs.

This project specifically focuses on analyzing the performance of controllers of IBRs in facing saturations. Different methods that are used for coping with the saturation of controllers are studied. Different anti-windup (AW) methods are implemented, and their performances are analyzed. A controller called Proxy Based Sliding Mode Controller (PBSMC) is implemented. PBSMC combines conventional PID controllers with nonlinear controller SMC to take advantage of both methods. It provides a systematic approach for addressing the saturation of PI controllers in facing large disturbances such as faults.

In the following sections the response of PV power plants in facing balanced and unbalanced faults are studied. The simulation results demonstrate utilizing appropriate methods for addressing the saturation of the controllers play an important role in enhancing PV power plants fault ride-through (FRT) capability and smoother transition into post-fault condition.

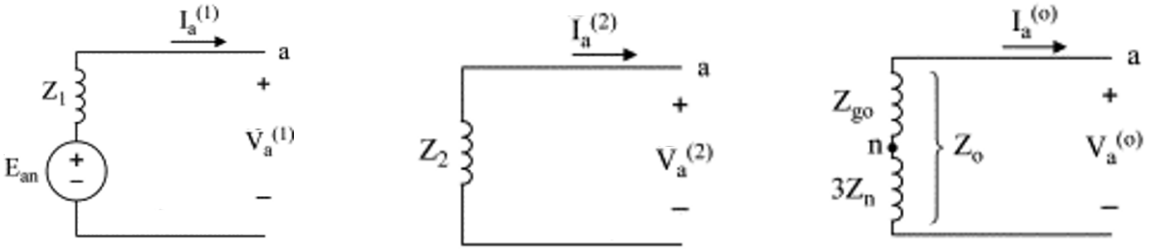
1.2 Fault Response of Inverter Based Resources

The fault response of conventional synchronous generators has been studied extensively in the literature and well-established models are developed as shown in Figure 1.1 (a) [1][2]. As Figure 1.1 (a) shows conventional synchronous generators are modeled in positive sequence networks by a voltage source behind the positive sequence impedance. In the negative and zero sequence networks, positive and negative sequence impedances are used to model synchronous generators fault response. In contrast to conventional synchronous generators, the fault response of inverter-based resources varies depending on the utilized technologies. Figure 1.1 (b). shows a generic model of IBRs with the current limiting feature. Before the fault occurrence, IBRs, according to their controllers, may inject a certain amount of active and reactive powers into the grid. During the fault, the controller reduces the output current such that the peak current value does not exceed the maximum tolerable overcurrent value.

Different grid codes define different requirements for IBRs fault responses. In [3][4] review of different grid codes is provided. Figure 1.2 [3] shows a typical grid code. As shown in Figure 1.2 (a) depending on the severity of the fault (i.e. percentage of voltage sag at the terminal of the inverter) different grid codes require inverters to remain connected to the grid with different durations. Moreover, inverters should inject reactive current into the grid. Figure 1.2 (b) indicates for every percent of the voltage drop, inverters should at least inject two percents of reactive currents if the voltage drop is between 50% to 90% of the nominal value of the terminal voltage.

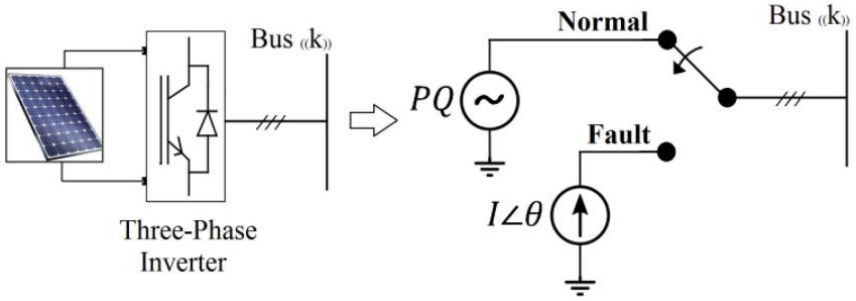
For voltage drops more than 50% of the nominal value of the terminal voltage, all nominal capacity of the inverter should be used to provide reactive current.

Faults in power grids could be balanced or unbalanced. In the following sections responses of inverters to balanced and unbalanced faults are discussed.



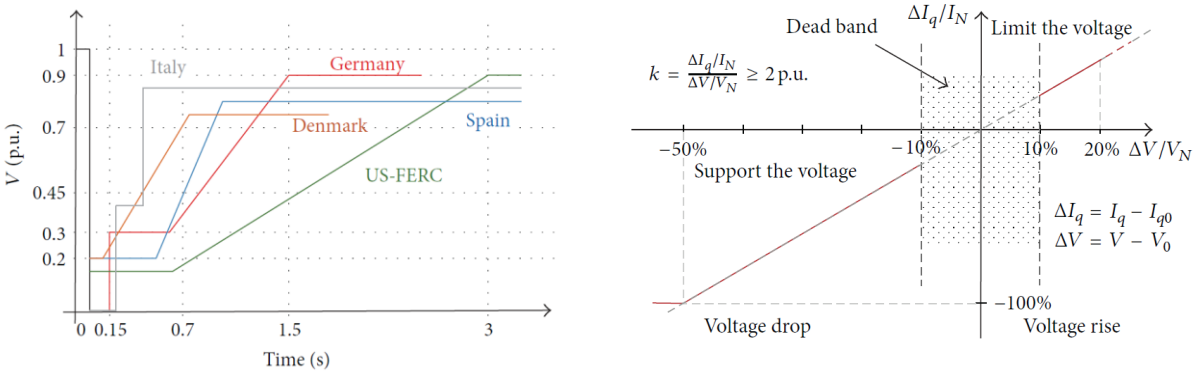
Positive sequence Negative sequence Zero sequence

(a)



(b)

Figure 1.1 (a) Model of conventional synchronous generators in sequence domain [1] (b) Generic equivalent model of IBRs [2]



(a) (b)

Figure 1.2 Grid codes requirements for fault ride through capability [3]

1.3 Fault Response of Inverters in Facing Balanced Faults

Figure 1.3 shows the implemented PV power plant. In this section it is assumed the fault is a symmetrical fault. The implemented controller has two control channels in d and q frames. It also has an inner current controller which controls the output current of the inverter. The outer controller provides the reference values to the inner current controller. Typically, in non-faulty condition, Iref-q =0 to allocate all capacity of the inverter to active power generated by the PV arrays. Iref-d is determined based on the voltage controller of the DC capacitor. At the DC side, by writing the KVL at the DC/DC converter the following holds [5]:

$$L\frac{di_b}{dt} = V_{in} - (1-U)V_{dc}) \tag{1.1}$$

Where U is the modulation control signal determined by the MPPT algorithm. L is the inductance in the dc link, i_b is the current flowing through the inductance, V_{in} is the voltage of the PV modules, V_{dc} is the voltage of the DC link capacitor.
The voltage dynamic at the capacitor is as follows:

$$C\frac{dV_{dc}}{dt} = (1-U)I_b - I_{dc} \tag{1.2}$$

Where C is capacitor in the dc link.
Also, by ignoring the power loss at the inverter

$$P_{ac} = P_{dc} \tag{1.3}$$

Where

$$P_{ac} = \frac{3}{2}(v_{id}i_d + v_{iq}i_q) \tag{1.4}$$

$$P_{dc} = V_{dc}I_{dc} \tag{1.5}$$

From (1.3) and (1.4), and (1.5):

$$I_{dc} = \frac{3}{2V_{dc}}(m_d\frac{V_{dc}}{2}i_d + m_q\frac{V_{dc}}{2}i_q) \tag{1.6}$$

By substituting (1.6) into (1.2), the following is derived:

$$C\frac{dV_{dc}}{dt} = (1-U)I_b - \frac{3}{4}(m_d i_d + m_q i_q) \tag{1.7}$$

Where P_{ac} and P_{dc} are power on the different side of inverters, P_{ac} is the power of inverter on the ac side of the system and P_{dc} is the power of inverter on the dc side of the system, $V_{dc}$is the voltage of the capacitor in the dc link and $i_{dc}$is the current flowing into the inverter from dc link. Also, m_d, $m_q$are modulating control signals for d and q channels.

According to (1.7), if the generated power by the PV arrays increases, the output current should be increased to ensure a fixed voltage value for the DC capacitor. Similarly, if the generated power by the PV arrays reduces, the output current should reduce too. This observation is used for generating Iref-d as shown in Figure 1.3 which utilizes a PI controller for this purpose.

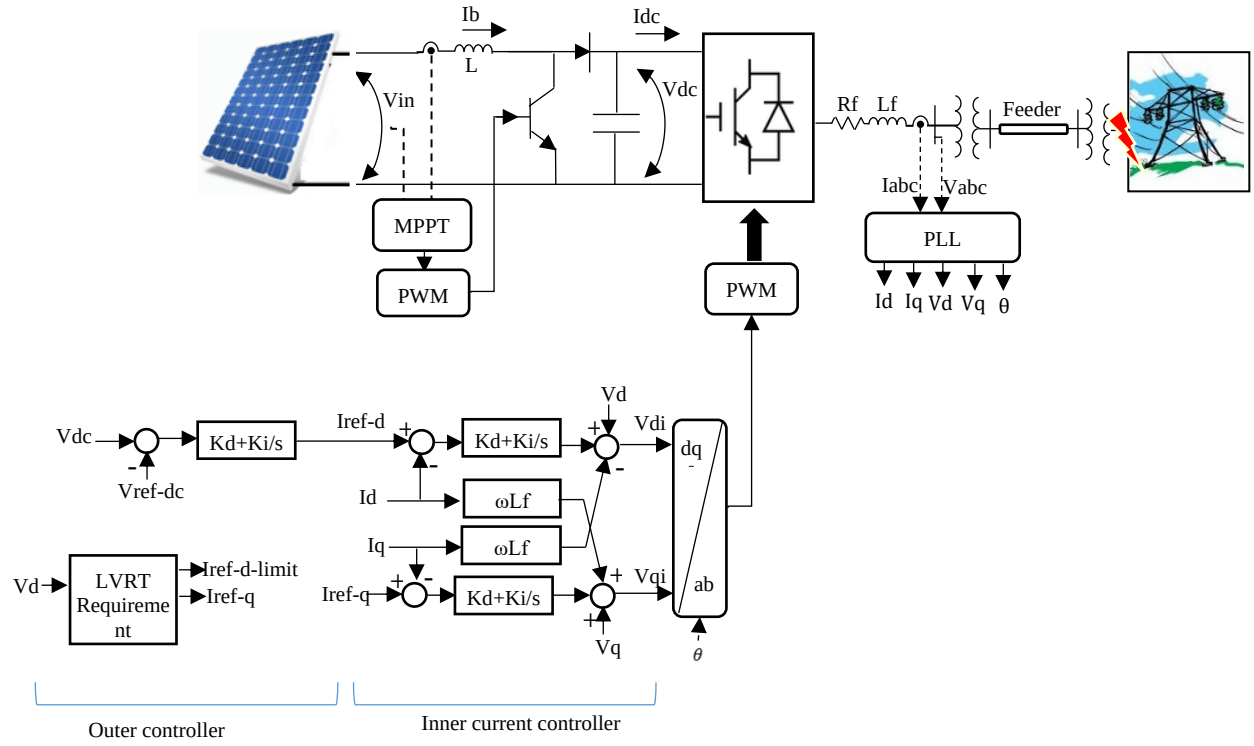


Figure 1.3 Schematic of PV power plant for symmetrical faults scenarios

1.3.1 Modeling of Constraints of Controllers

An important aspect of the controllers is controllers saturation when the control output is limited by the inverter limits. The following constraint holds for the inverter output current:

$$\sqrt{{I_d}^2 + {I_q}^2} \leq I_{max} \tag{1.8}$$

Where I_d and I_q are the current of the converter in d and q frame and I_{max} is the maximum current can flow in the inverter. Typically, $I_{max} = 1.2I_{nominal}$ which $I_{nominal}$ is the nominal current of the inverter. Also, the following holds for V_{di} and V_{qi} in Figure 1.3:

$$\sqrt{{V_{di}}^2 + {V_{qi}}^2} \leq V_{max} \tag{1.9}$$

Where V_d and V_q are the voltages of the inverter in d and q frames and V_{max} is the maximum voltage of the inverter.

As Figure 1.4 (a)[6] shows, equation (1.9) represents an area indie a circle with the radius of V_{max}. There are different methods for enforcing the limits. In [6] detailed discussions of the methods are provided. One common approach is rectangular approximation or boxed constraints.

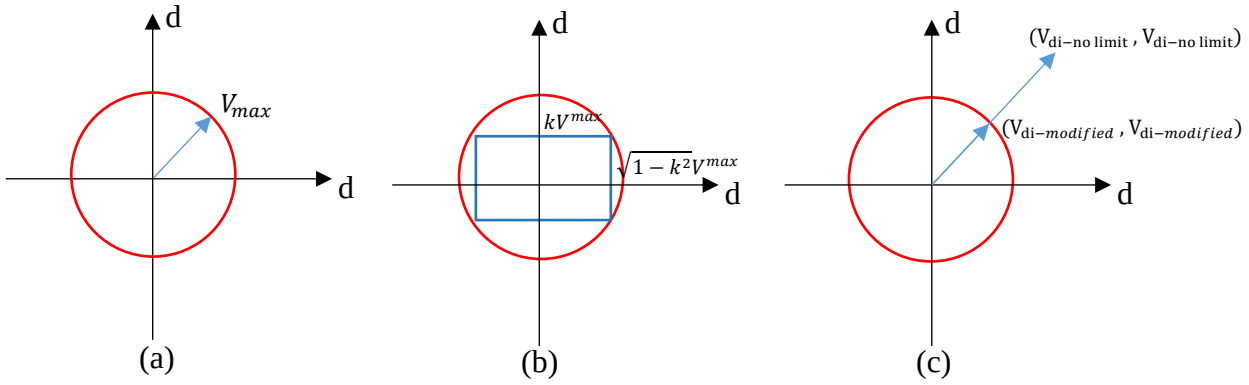


Figure 1.4 Different approaches for enforcing inverter constraints[6]

Figure 1.4 (b)[6] shows the structure of this approximation. It is assumed

$$V_{qi}{}^{max} = kV^{max} \tag{1.10}$$

Where k is a factor $0 \leq k \leq 1$. According to (1.9) and (1.10), the following holds:

$$V_{di}{}^{max} = \sqrt{1-k^2}V^{max} \tag{1.11}$$

Therefore, instead of (1.9) the following constraints are used:

$$\begin{aligned} -V_{qi}{}^{max} \leq V_{qi} \leq V_{qi}{}^{max} \\ -V_{di}{}^{max} \leq V_{di} \leq V_{di}{}^{max} \end{aligned} \tag{1.12}$$

The advantage of boxed constraints approximation is that the limits are fixed constant values. Therefore, the controller design and implementation are easier. However, it does not fully utilize the available capacity of the inverter as shown in Figure 1.4 (b)[6].

Another approach is Maintaining the Same Ratio approach. In this approach at first the control constraints are ignored, and control values of d and q channels are calculated as $V_{di-no\ limit}$ and $V_{qi-no\ limit}$. No further action is needed, if the following holds,

$$\sqrt{V_{di-no\ limit}{}^2 + V_{qi-no\ limit}{}^2} \leq V_{max} \tag{1.13}$$

However, if (1.13) does not hold, modified values of d and q channels should be calculated as $V_{di-modified}$ and $V_{qi-modified}$. In Maintaining Same Ratio approach, the following should hold:

$$\frac{V_{di-no\ limit}}{V_{qi-no\ limit}} = \frac{V_{qi-modified}}{V_{qi-modified}} \tag{1.14}$$

Equation (1.14) can be interpreted as Figure 1.4-(c)[6]. $V_{di-modified}$ and $V_{qi-modified}$ should satisfy the relationship in (1.14) and also the following relationship:

$$\sqrt{{V_{di-modified}}^2 + {V_{qi-modified}}^2} = V_{max} \tag{1.15}$$

One solution is as follows:

$$V_{di-modified} = \frac{V_{di-no\ limit}}{\sqrt{{V_{di-no\ limit}}^2 + {V_{qi-no\ limit}}^2}} V_{max} \tag{1.16}$$

$$V_{qi-modified} = \frac{V_{qi-no\ limit}}{\sqrt{{V_{di-no\ limit}}^2 + {V_{qi-no\ limit}}^2}} V_{max} \tag{1.17}$$

The advantage of the above approach is that the full capacity of the inverter is utilized. However, it requires changing the constraints in real-time which complicates the control design and implementation.

Another approach which is commonly used in IBRs, and is also implemented in this project, is assigning priority to one of the control channels. In this approach like the previous method, first the limits on the control channels are ignored and $V_{di-no\ limit}$ and $V_{qi-no\ limit}$ are calculated. Assuming q channel is the control channel with a higher priority, the following procedure is followed:

If $V_{qi-no\ limit} \geq V_{max}$, then
$V_{qi-modified} = V_{max}$ and $V_{di-modified} = 0$
If $V_{qi-no\ limit} < V_{max}$, then
$V_{qi-modified} = V_{qi-no\ limit}$
If $V_{di-no\ limit} < \sqrt{V_{max}^2 - {V_{qi-no\ limit}}^2}$, then
$V_{di-modified} = V_{di-no\ limit}$
If $V_{di-no\ limit} \geq \sqrt{V_{max}^2 - {V_{qi-no\ limit}}^2}$, then
$V_{di-modified} = \sqrt{V_{max}^2 - {V_{qi-no\ limit}}^2}$ (1.18)

Following similar approach, the grid code requirement in Figure 1.2 (b), and considering q channel has the higher priority, the following can be written:

$I_{q-check} = 2(1 - V_d)I_N$

If $V_d > 0.9$, then

$I_{q-modified} = I_{q0}$ and $I_{d-modified} = I_{d0}$

If $V_d \leq 0.9$, then

If $I_{q-check} \geq I_{max}$, then

$I_{q-modified} = I_{max}$, $I_{d-modified} = 0$

If $I_{q-check} < I_{max}$, then

$I_{q-modified} = I_{q-check}$

If $I_{d-no\ limit} \geq \sqrt{I_{max}^2 - I_{q-check}^2}$

$I_{d-modified} = \sqrt{I_{max}^2 - I_{q-check}^2}$ (1.19)

If $I_{d-no\ limit} < \sqrt{I_{max}^2 - I_{q-check}^2}$

$I_{d-modified} = I_{d-no\ limit}$

The common approach in facing constraints in the controllers channels is utilizing anti-windup (AW) strategies. When a PI controller faces limits, the integral part accumulates errors terms. If no approaches are used to address the problem, the time the controller remains in the saturation mode increases which degrades the response and even may lead to instability of the controller.

There are several AW approaches that are used in power systems such as PI conditional, Dead zone, tracking method, and track gain method which will be discussed in the later sections. These methods help to reduce the saturation effects on integral part of the controller. Saturation happens when the integral action accumulates error.

The proper tuning of AW methods is a challenging problem. Tuning AW parameters is a heuristic procedure. Therefore, methods that can address the saturation of PIs while can be tuned systematically is of special interest. Specifically in this project, a method called proxy-based sliding mode control (PBSMC) method is used which is developed in [7][8]. PBSMC interfaces nonlinear sliding mode control and PID control by using a virtual objective (proxy) so that the resulting control law has the advantages of each approach while addressing the saturation problem of PI controllers.

1.3.2 Methods for Handling Controllers Saturations

In the following section a brief review of the AW methods that have been implemented in power systems and presented in [9] are reviewed. The methods are implemented on a simulated PV power plant in Matlab Simulink which will be discussed in later sections.

Anti-windup PI with dead zone method

Figure 1.5 [9] shows the schematic of this method. The integral value is compared with the dead zone limit. If this value is larger than the limit, the value will be reduced, otherwise, no changes are made to the value.

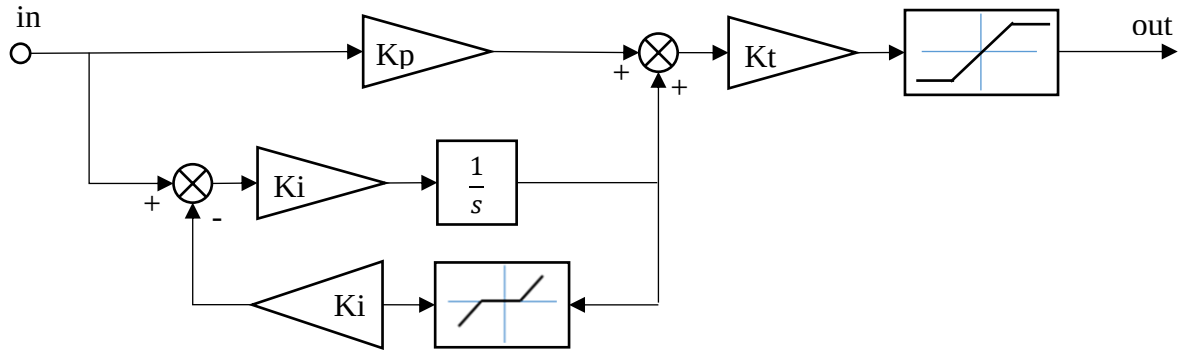


Figure 1.5 Anti-Windup PI with dead zone method

Anti-windup PI conditioned method

Figure 1.6 [9] shows the schematic of this method. In this scheme, if the values between the input and output of the saturation block are different, the integral value is held in the latest value to decrease the saturation effects by not letting the integral part accumulate the error. In this method, a switch is used to ensure that if any difference between the input and output of saturation block appears, the input of the integral part is set to zero. This method is used in IEEE Std. 421.5-2016. Although it has a simple structure and commonly used, there are applications that it does not operate properly, and alternative solutions have been proposed to address the shortcomings [10]

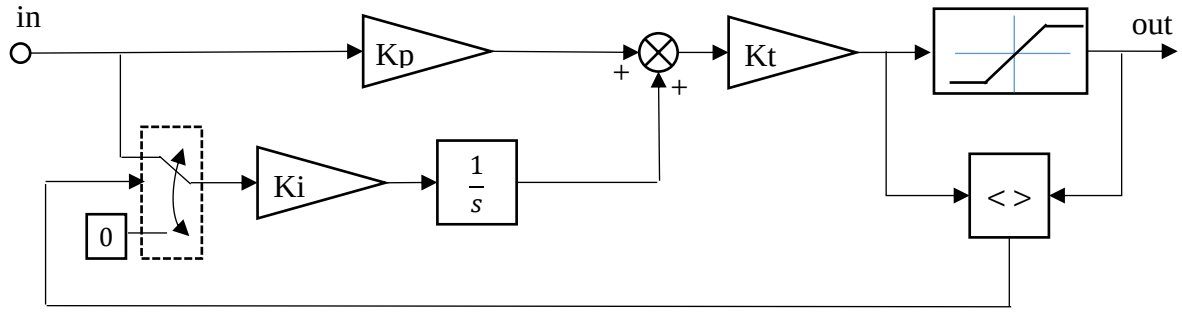


Figure 1.6 Anti Widup PI conditioned method

Anti-windup PI tracking method

Figure 1.7 [9] shows the schematic of this method. In this scheme, the difference between the input and output of the saturation block is used to reduce the effect of error accumulation in the integral part. In this method, typically overshoot in the response appears, but the time the system remains in the saturation decreases.

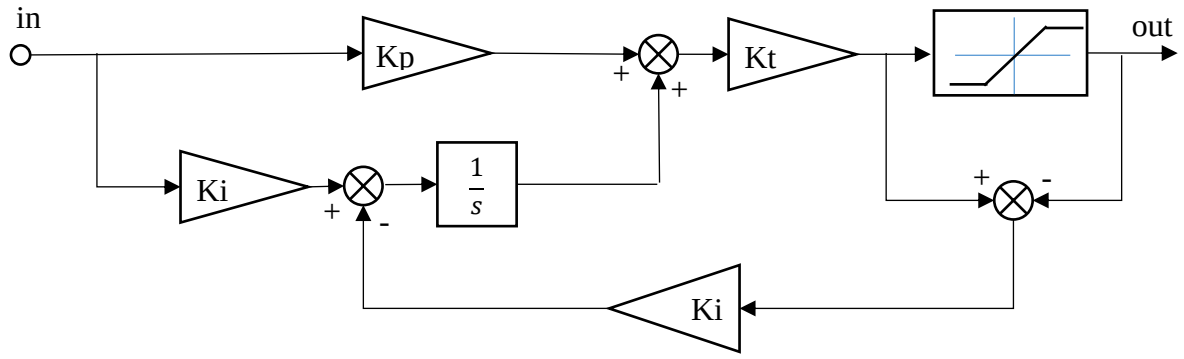


Figure 1.7 Anti-Windup PI tracking method

Anti-windup PI tracking with gain method

Figure 1.8 [9] shows the schematic of this method. This method is similar to the previous method but uses another gain in the feedback loop to improve the results. The gain G is between 1 and zero.

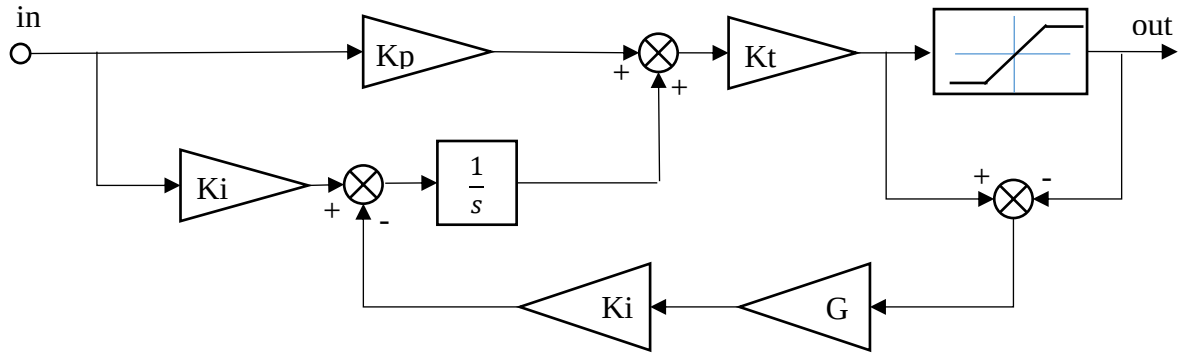


Figure 1.8 Anti-Windup PI tracking with gain method

Proxy-based sliding mode control (PBSMC)

In [7][8] a controller called PBSMC is proposed that combines PID controllers and SMC. PBSMC provides accurate and fast-tracking feature during normal condition while provides smooth resuming to the desired trajectory in facing large disturbances. Therefore, there is no need to make the PID controller unnecessarily slower. Moreover, compared to conventional AW methods that are heuristic approaches, PBSMC provides a more systematic approach for managing the post-saturation condition. Figure 1.9 shows the overall idea of the PBSMC. The PID controller interfaced to the SMC though a virtual object (proxy). The overall PID controller can be written as follows:

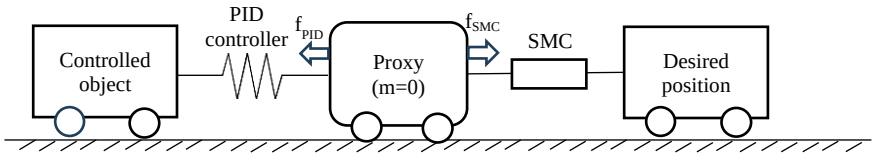


Figure 1.9 Schematic of PBSMC

$$f_{PID} = k_p.(x_p - x) + k_i.\int_0^t (x_p - x)\,dT + k_d.\frac{d}{dt}(x_p - x) \tag{1.20}$$

where, x and x_p denote the position of controlled object and position of the proxy, respectively. k_p, k_i and k_d are proportional, integral and derivative gains of PID controller, respectively. The objective of the SMC is to bring the position of the proxy to the desired position according to the sliding surface as follows:

$$S_{PBSMC} = K\frac{d}{dt}(x_d - x_p) + (x_d - x_p) \tag{1.21}$$

Where x_d is the desired position of the controlled object Therefore, the control law of the SMC becomes as follows:

$$f_{SMC} = F.sgn(S_{PBSMC}) = F.sgn(K\frac{d}{dt}(x_d - x_p) + (x_d - x_p)) \tag{1.22}$$

Where S_{PBSMC} is sliding surface of PBSMC
In Figure 1.9 , the motion equation for the proxy (i.e. virtual object) is as follows:

$$m.\frac{d^2x_p}{dt} = f_{smc} - f_{PID} \tag{1.23}$$

where, m is the mass of the proxy and is assumed to be zero. Therefore, the following holds:

$$f_{smc} = f_{PID} \tag{1.24}$$

In [11], the above equations are utilized and after using a series of mathematical relations, the PBSMC is developed as shown in Figure 1.10 [11]. The λ is a gain that can determine the speed of the response of the system.
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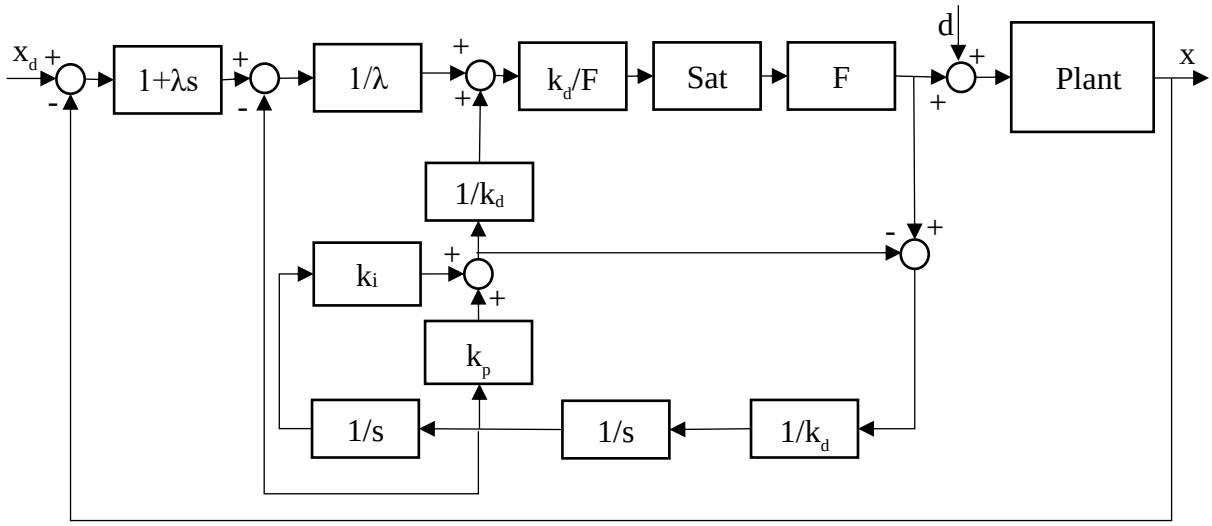

Figure 1.10 Proxy-based sliding mode control structure

1.3.3 Performance of Controllers in Different Hypothetical Plant Models

In this section to investigate the performance of different AW methods, several hypothetical plant models are considered. Then, the methods are applied to a PV power plant.

CASE 1: A plant model of $\frac{10}{s^2+10s+5}$ is considered and the PI parameters are K_p=10, K_i=4 and the plant input limit value is 14, and the reference is a step function from zero to five. The results are shown in Figure 1.11 and Figure 1.12. As can be seen in the simulated results, PBSMC has either similar or better response compared to other methods.

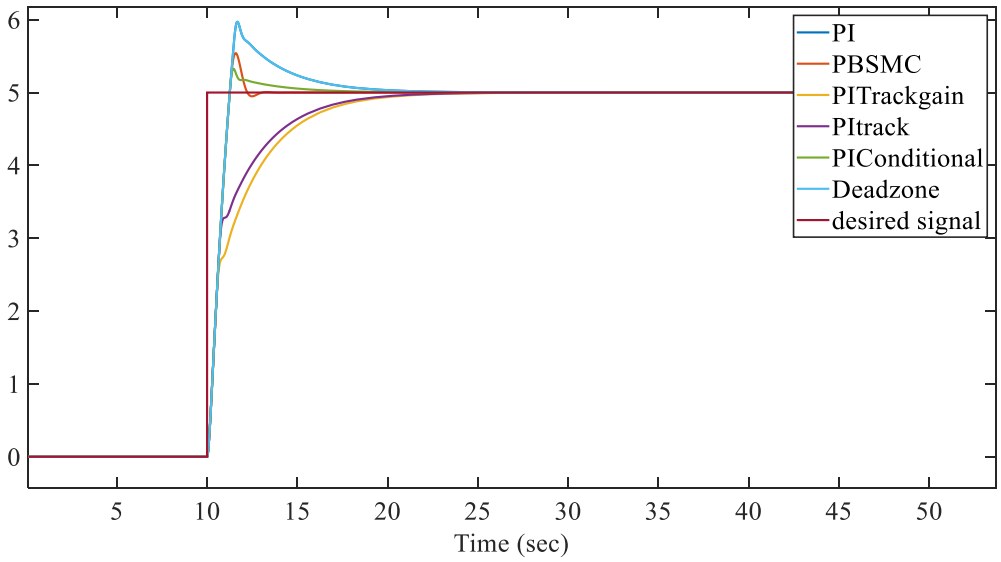

Figure 1.11 Comparison of different controllers in CASE 1

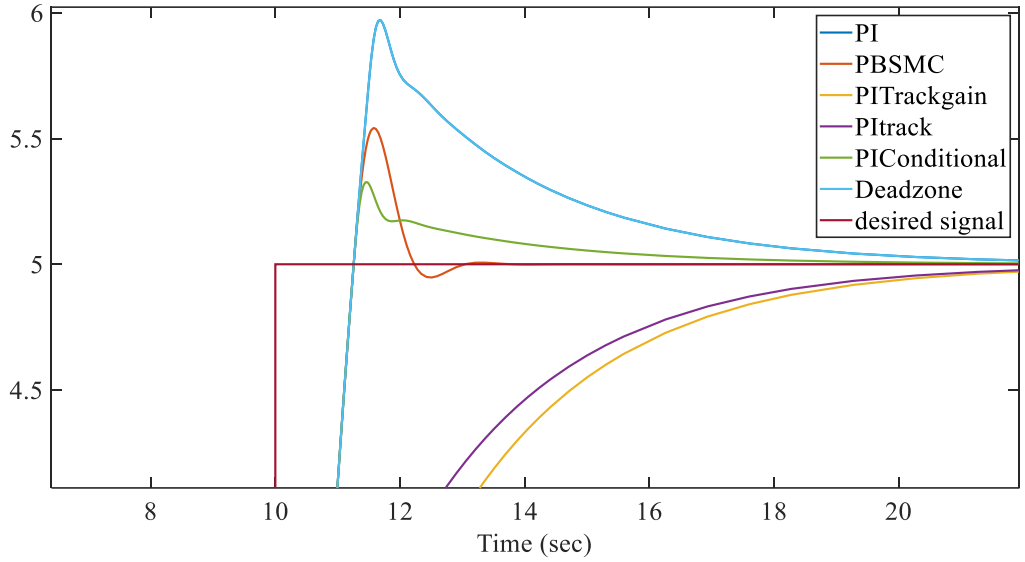

Figure 1.12 Comparison of different controllers in CASE 1, zoomed values

One advantage of the PBSMC is it has a systematic approach for the analysis of the impact of the controller parameters (i.e. λ) which makes the use of controller systematic.

CASE 2: The second considered plan model is $\frac{180}{s^2+14s+41}$. The controller parameters are K_p=30, K_i=20, Kd=0.6 and the input limit is 23 and the refrence is a step from 0 to 100 at t=10 second. The results are shown in Figure 1.13 and Figure 1.14. Similar to the previous case PBSMC controller has similar or better performance compared to other methods.

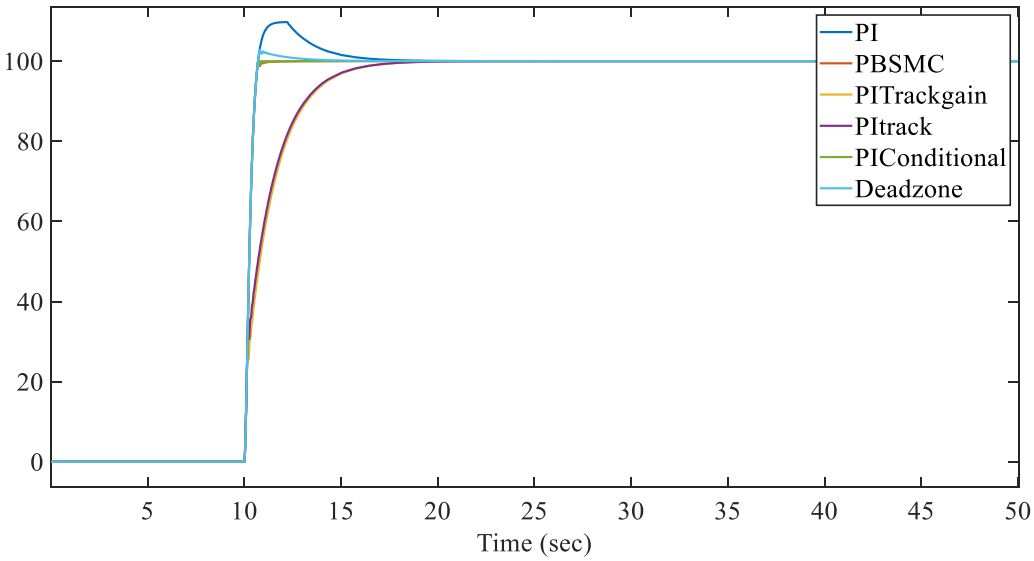

Figure 1.13 Comparison of different controllers in CASE 2

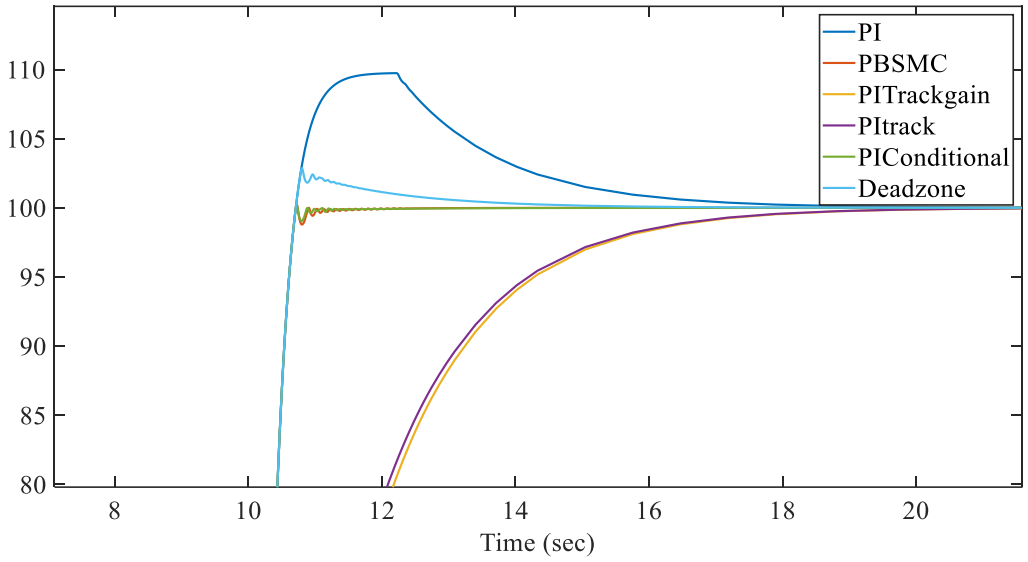

Figure 1.14 Comparison of different controllers in CASE 2, zoomed values

1.3.4 Performance of Controllers in PV Power Plant: Balanced Fault Cases

The power plan shown in Figure 1.3 is simulated in Matlab/Simulink and different AW methods are applied to the controller. According to the case study results, the limit on the PI controller of DC capacitor is influential. This is because during the fault, the controllers of the inverter follows the fault ride through requirements which requires injecting reactive current. This limits the available capacity for injecting Id which directly affects the voltage of the DC capacitor. To investigate the performance of different approaches, different fault scenarios are studies.

CASE 1: A three-phase fault occurs between 1.5 and 1.6667 seconds with a fault resistance of 0.001 ohms and a ground resistance of 0.01 ohms. This fault causes saturation in the Id channel because the Iq should be injected into the system. Figure 1.15 to Figure 1.17 show the results in this case. Note in the figures “PI” means no AW method is used which is not a realistic condition. It is only reported to show the impact of the saturation on the results.

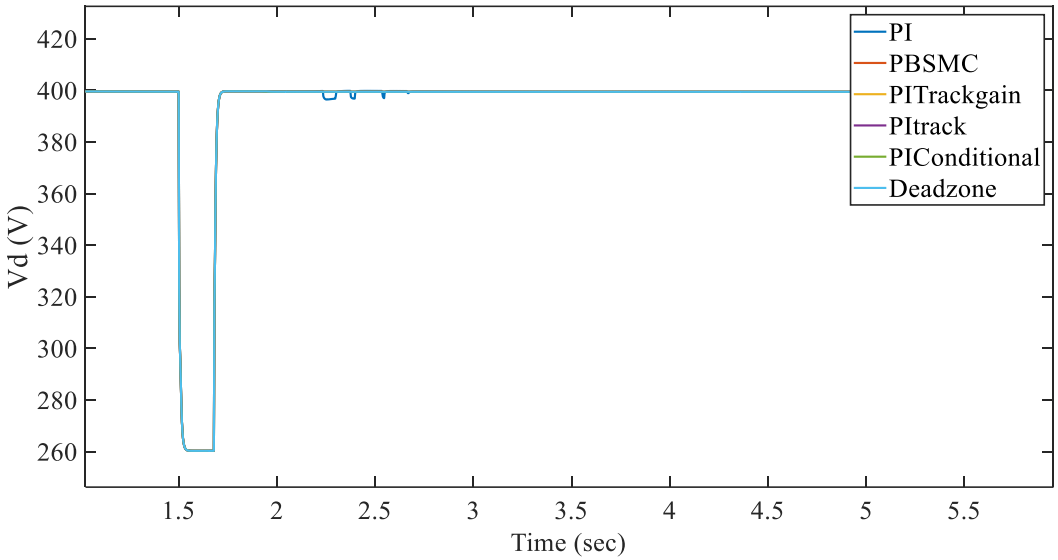

Figure 1.15 Vd for the balanced fault CASE 1

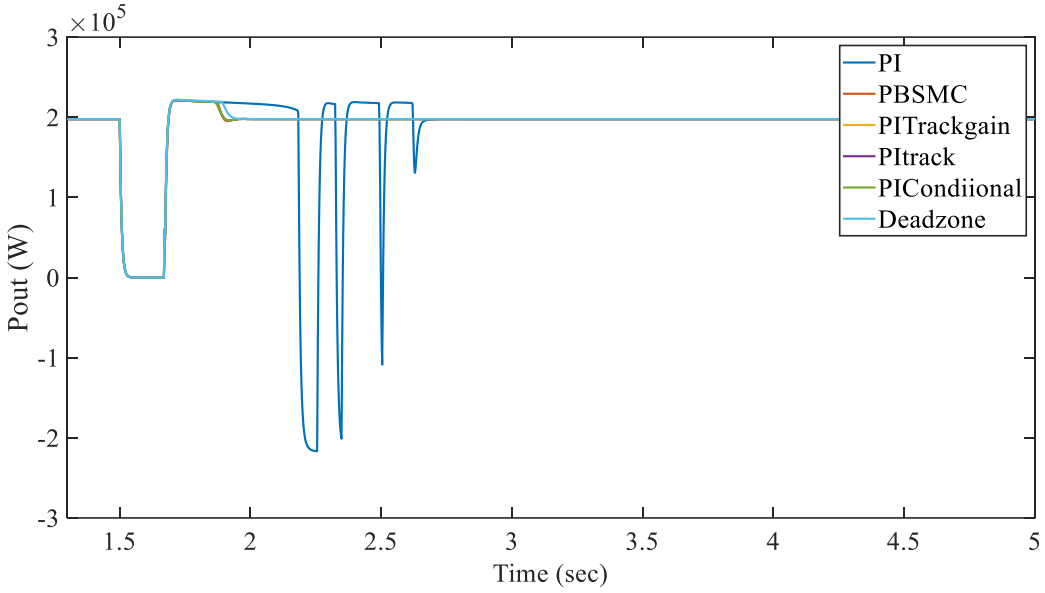

Figure 1.16 Pout for the balanced fault CASE 1

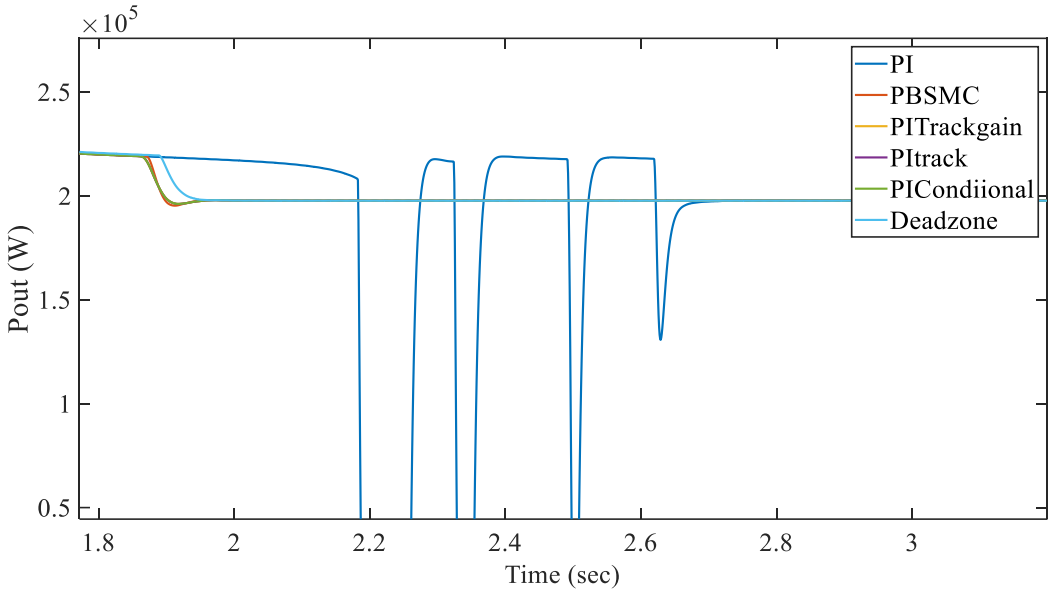

Figure 1.17 Pout zoomed on the saturation time for the balanced fault CASE 1

CASE 2: Compared to the previous case, the fault resistance is changed to 20 ohms. Figure 1.18 to Figure 1.20 show the results. In this case the voltage level does not drop like the previous case, and the controllers get out of saturation sooner than the previous case.

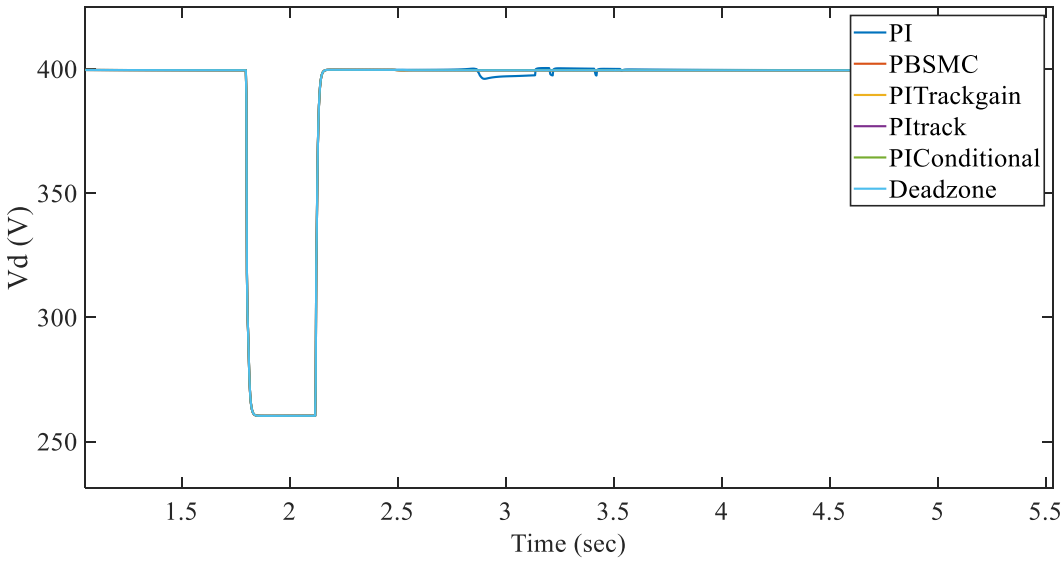

Figure 1.18 Vd for the balanced fault CASE 2

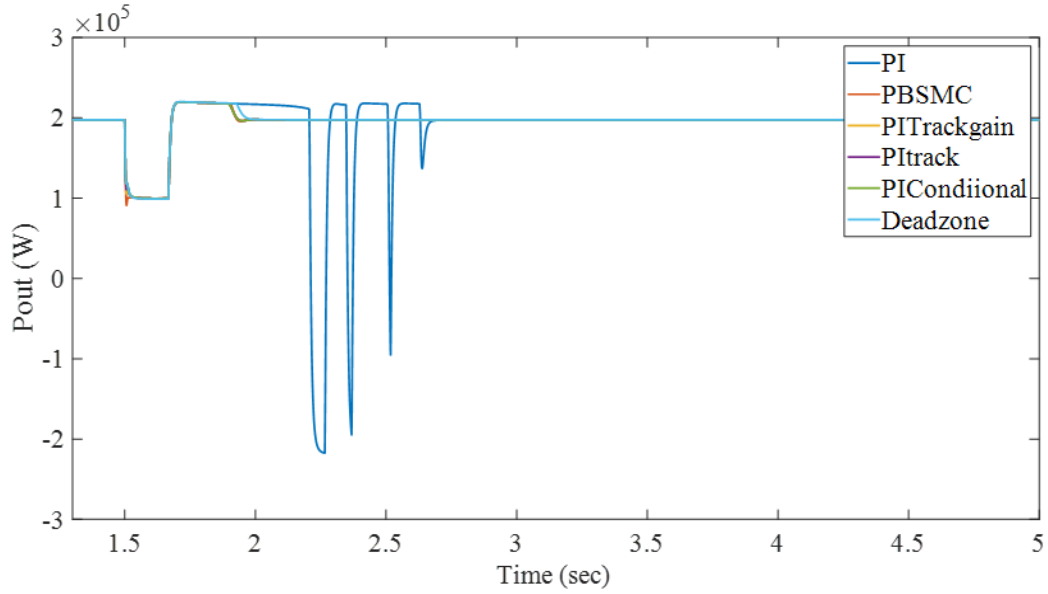

Figure 1.19 Pout for the balanced fault CASE 2

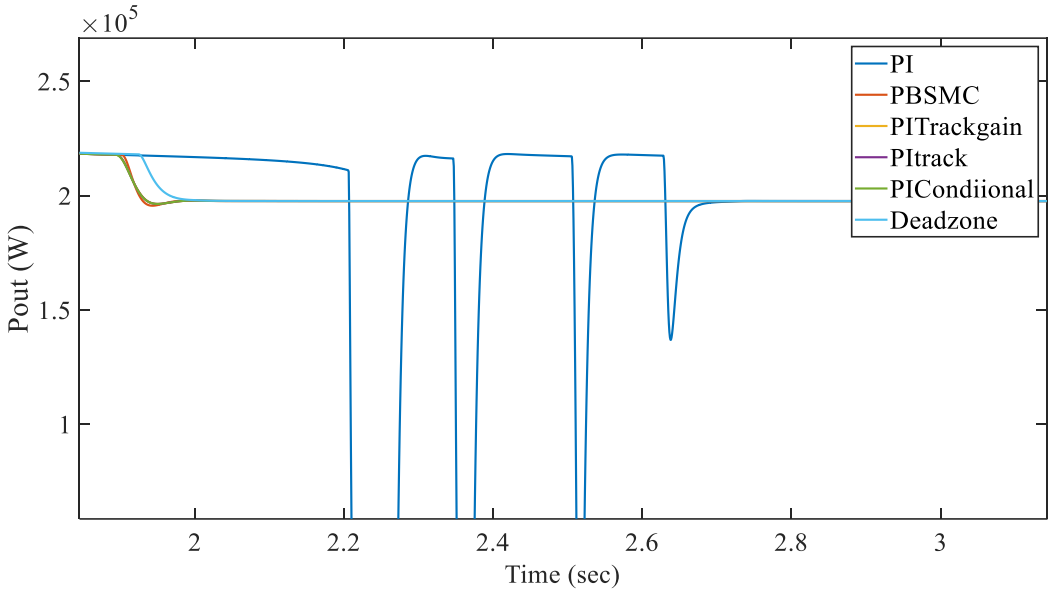

Figure 1.20 Pout zoomed on the saturation time for the balanced fault CASE 2

CASE 3: In this case, the fault starts at 1.8 seconds and lasts until 2.12 seconds, twice the duration of the previous scenario. Furthermore, the ground resistance is 0.01 ohms, and the fault resistance is 20 ohms. The simulation results are presented in Figure 1.21 to Figure 1.23.

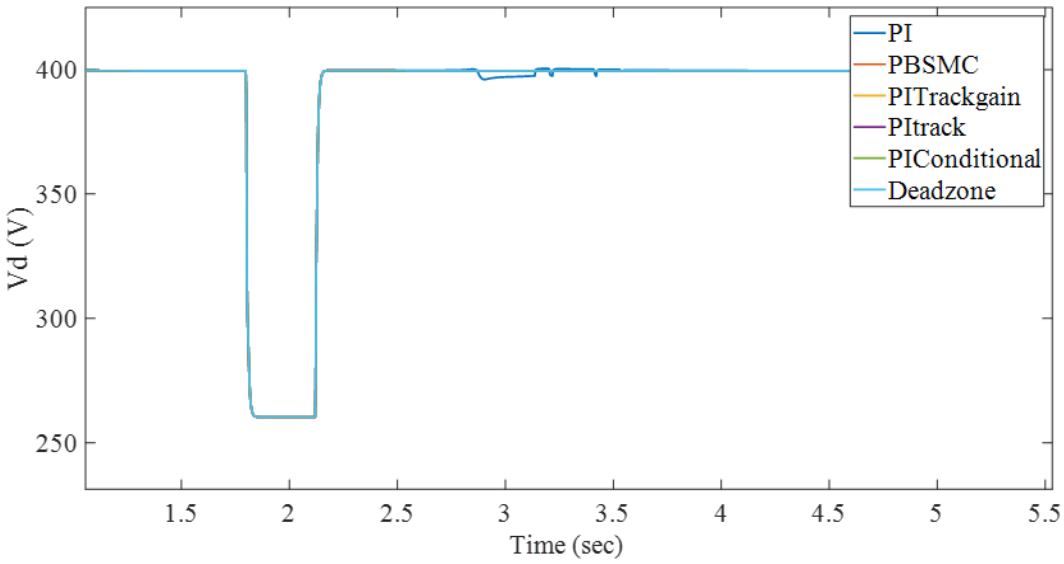

Figure 1.21 Vd for the balanced fault CASE 3

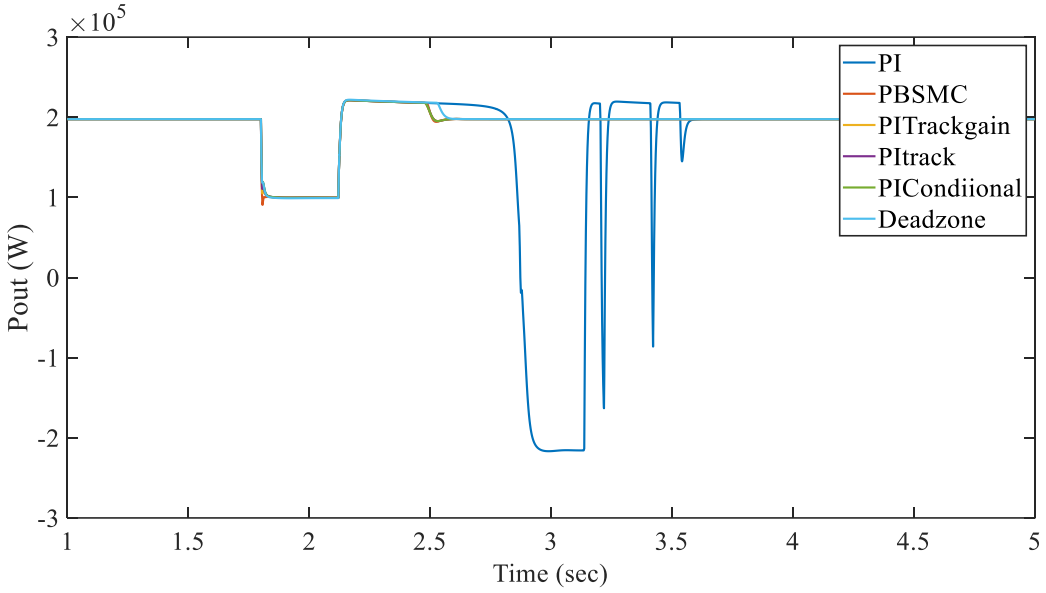

Figure 1.22 Pout for the balanced fault CASE 3

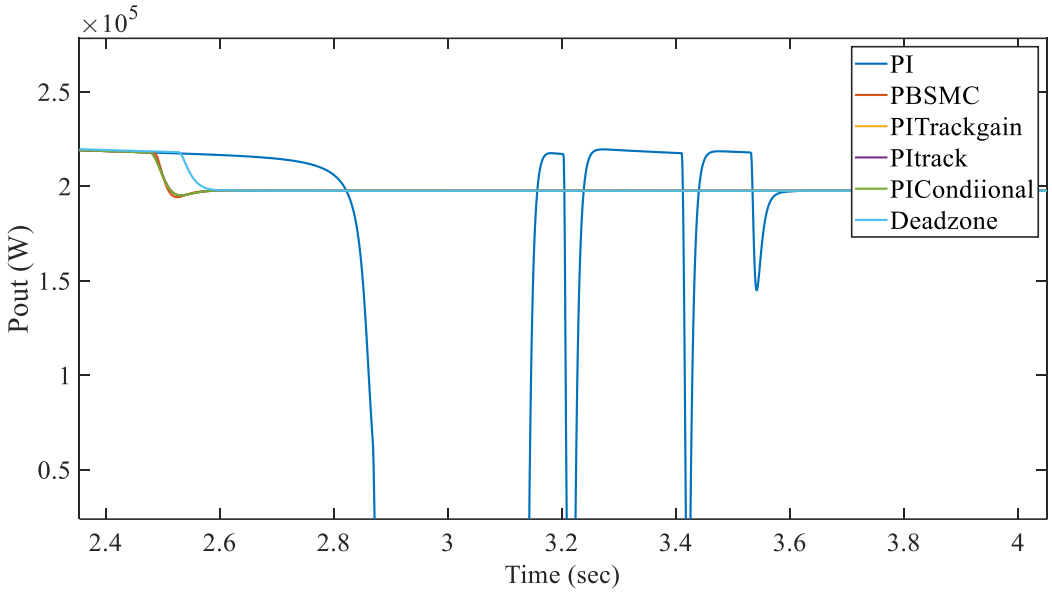

Figure 1.23 Pout zoomed on the saturation time for the balanced fault CASE 3

As the results show AW methods significantly improve the transitioning of the PV power plant to the post fault condition. Moreover, according to the simulation results, PBSMC method has either same or better performance compared to the AW methods. However, tuning the AW methods involves heuristic approaches. In contrast, tuning PBSMC is more systematic.

1.4 Fault Response of Inverters in Facing Unbalanced Faults

When an unbalanced fault occurs, the voltage and current signals become unbalanced. Therefore, the conventional synchronous reference frame phase-locked loop (SRF-PLL) becomes ineffective due to presence of double frequency oscillations. To explain this issue, Figure 1.24 and Figure 1.25 are used. In Figure 1.24 a three-phase balanced positive sequence voltage signals are applied to the SRF-PLL PLL. In Figure 1.25 a three-phase balanced negative sequence voltage signals are applied to the SRF-PLL PLL. As shown in Figure 1.24 and Figure 1.25 the vector derived by the Clarke transformation in Figure 1.24 rotates in the opposite direction of that of Figure 1.25. In the case of unbalanced fault, such as phase to phase or phase to ground faults, both positive and negative sequence components appear at the same time in the signals. Note that due to the configuration of the interfacing transformer, the zero-sequence component is not observed by the inverter controller.

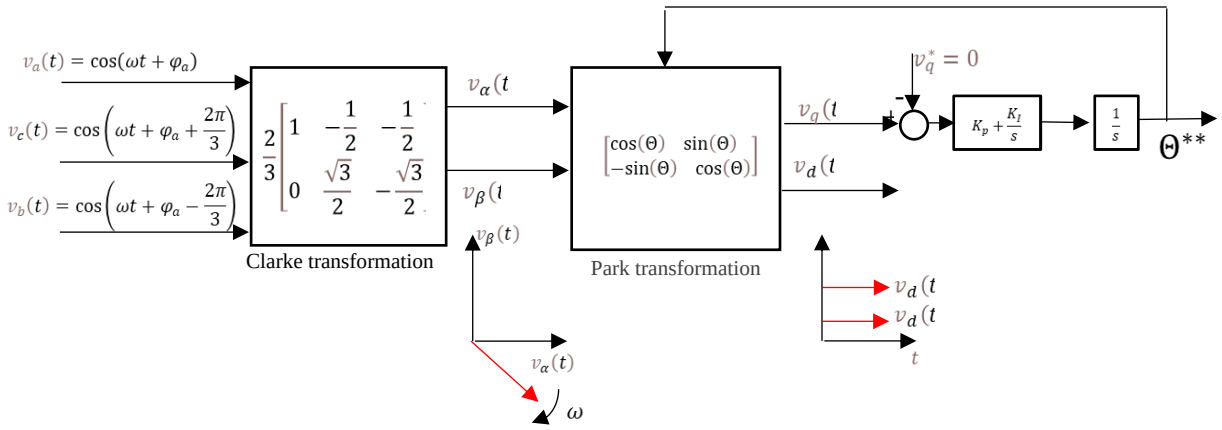

Figure 1.24 Three phase positive-sequence signal transformation to the dq frame

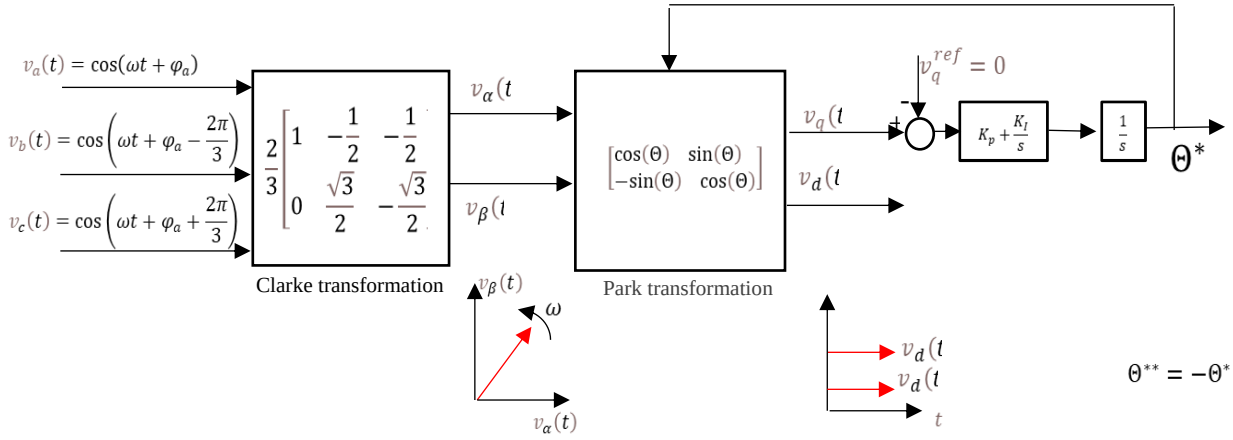

Figure 1.25 Three phase positive-sequence signal transformation to the dq frame

Therefore, the terminal voltage can be written as follows:

$$\begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix} = \begin{bmatrix} v_a^+(t) \\ v_b^+(t) \\ v_c^+(t) \end{bmatrix} + \begin{bmatrix} v_a^-(t) \\ v_b^-(t) \\ v_c^-(t) \end{bmatrix} = \begin{bmatrix} V_{max}cos(\omega t + \varphi_a^+) \\ V_{max}cos(\omega t + \varphi_a^+ - \frac{2\pi}{3}) \\ V_{max}cos(\omega t + \varphi_a^+ + \frac{2\pi}{3}) \end{bmatrix} + \begin{bmatrix} V_{max}cos(\omega t + \varphi_a^-) \\ V_{max}cos(\omega t + \varphi_a^- + \frac{2\pi}{3}) \\ V_{max}cos(\omega t + \varphi_a^- - \frac{2\pi}{3}) \end{bmatrix} \quad (1.25)$$

If the Park transformation with $\theta = \theta^*$is applied, the following is derived

$$\begin{bmatrix} v_{d+} \\ v_{q+} \end{bmatrix} = \begin{bmatrix} v_{d+}^* \\ v_{q+}^* \end{bmatrix} + \begin{bmatrix} \cos(2\theta^*) & \sin(2\theta^*) \\ -\sin(2\theta^*) & \cos(2\theta^*) \end{bmatrix} \begin{bmatrix} \bar{v}_{d-} \\ \bar{v}_{q-} \end{bmatrix} \quad (1.26)$$

If the Park transformation with $\theta = -\theta^*$is applied, the following is derived

$$\begin{bmatrix} v_{d-} \\ v_{q-} \end{bmatrix} = \begin{bmatrix} v_{d-}^{*} \\ v_{q-}^{*} \end{bmatrix} + \begin{bmatrix} \cos(-2\theta^{*}) & \sin(-2\theta^{*}) \\ -\sin(-2\theta^{*}) & \cos(-2\theta^{*}) \end{bmatrix} \begin{bmatrix} \bar{v}_{d+} \\ \bar{v}_{q+} \end{bmatrix} \quad (1.27)$$

Where $v_{d+}^{*}, v_{d-}^{*}, v_{q+,}^{*} v_{q-}^{*}$ are value of positive and negative sequence voltage at the inverter terminal in dq reference frame.

One way to extract $\begin{bmatrix} v_{d-}^{*} \\ v_{q-}^{*} \end{bmatrix}$ in (1.27) or $\begin{bmatrix} v_{d+}^{*} \\ v_{q+}^{*} \end{bmatrix}$ in (1.26), is using a low pass filter to eliminate the second harmonic components. However, it makes the PLL extremely slow which deteriorates its performance in tracking fast changing disturbances. To address this issue, decoupled double synchronous reference frame-PLL (DDSRF PLL) [12] is implemented. Figure 1.25 shows the overall structure of the DDSRF PLL. In DDSRF PLL the decupling is performed as follows:
According to (1.26) and (1.27)

$$\begin{bmatrix} v_{d+}^{*} \\ v_{q+}^{*} \end{bmatrix} = \begin{bmatrix} v_{d+} \\ v_{q+} \end{bmatrix} - \begin{bmatrix} \cos(2\theta^{*}) & \sin(2\theta^{*}) \\ -\sin(2\theta^{*}) & \cos(2\theta^{*}) \end{bmatrix} \begin{bmatrix} \bar{v}_{d-} \\ \bar{v}_{q-} \end{bmatrix} \quad (1.28)$$

And

$$\begin{bmatrix} v_{d-}^{*} \\ v_{q-}^{*} \end{bmatrix} = \begin{bmatrix} v_{d-} \\ v_{q-} \end{bmatrix} - \begin{bmatrix} \cos(-2\theta^{*}) & \sin(-2\theta^{*}) \\ -\sin(-2\theta^{*}) & \cos(-2\theta^{*}) \end{bmatrix} \begin{bmatrix} \bar{v}_{d+} \\ \bar{v}_{q+} \end{bmatrix} \quad (1.29)$$

Equations (1.28) and (1.29) can be represented in block diagrams as Figure 1.26[13]

When an unbalanced fault occurs, the active and power of inverter can be written as follows[14]:

$$\begin{aligned} P &= P_0 + P_c \cos(2\omega t) + P_s sin\,(2\omega t) \\ Q &= Q_0 + Q_c \cos(2\omega t) + Q_s sin\,(2\omega t) \end{aligned} \quad (1.30)$$

P_0 and Q_0 are the average values of instantaneous power and the P_c, P_s, Q_c, Q_s are oscillatory term of power in unbalanced situation.

$$\begin{aligned} P_0 &= 1.5 \times \left(v_d^{+} i_d^{+} + v_q^{+} i_q^{+} + v_d^{-} i_d^{-} + v_q^{-} i_q^{-}\right) \\ P_c &= 1.5 \times \left(v_d^{+} i_d^{-} + v_q^{+} i_q^{-} + v_d^{-} i_d^{+} + v_q^{-} i_q^{+}\right) \\ P_s &= 1.5 \times \left(v_q^{-} i_d^{+} - v_d^{-} i_q^{+} - v_q^{+} i_d^{-} + v_d^{+} i_q^{-}\right) \\ Q_0 &= 1.5 \times \left(v_q^{+} i_d^{+} - v_d^{+} i_q^{+} + v_q^{-} i_d^{-} - v_d^{-} i_q^{-}\right) \\ Q_c &= 1.5 \times \left(v_q^{+} i_d^{-} - v_d^{+} i_q^{-} + v_q^{-} i_d^{+} + v_d^{-} i_q^{+}\right) \\ Q_s &= 1.5 \times \left(v_d^{+} i_d^{-} + v_q^{+} i_q^{-} - v_d^{-} i_d^{+} - v_q^{-} i_q^{+}\right) \end{aligned} \quad (1.31)$$

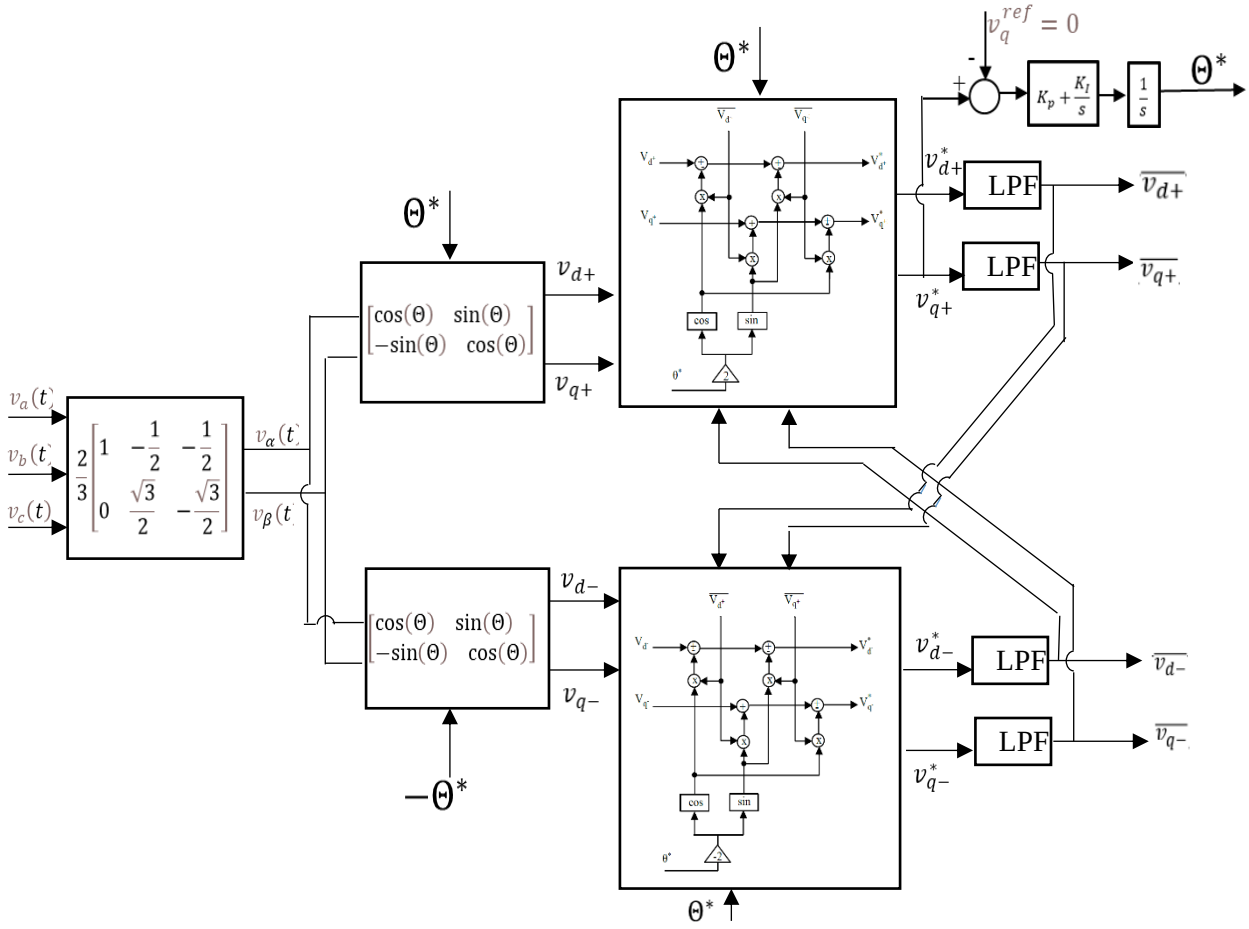

Figure 1.26 Schematic of decoupled double synchronous reference frame-PLL (DDSRF PLL)

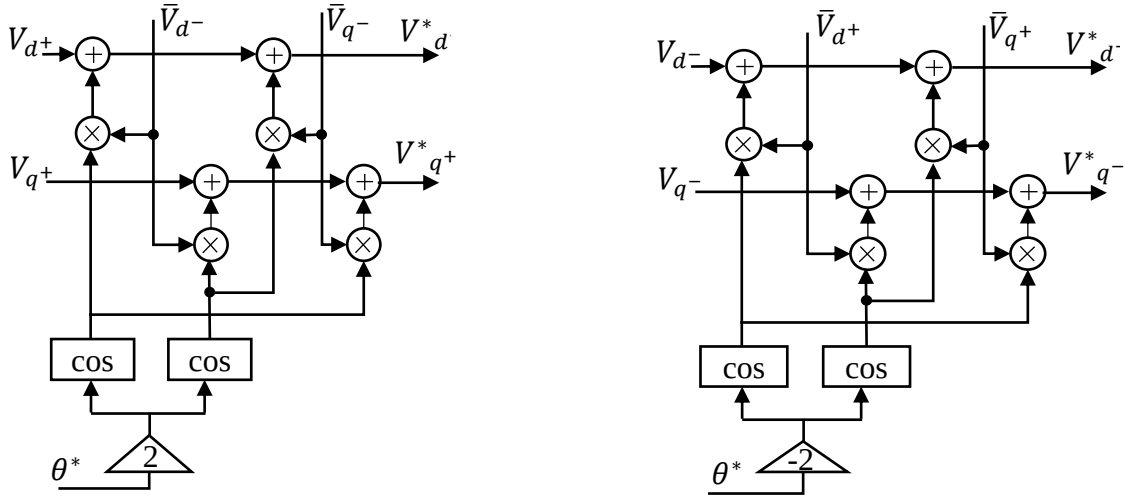

Figure 1.27 Block diagram of the decompiling process for extracting sequence component in DDSRF PLL [13]

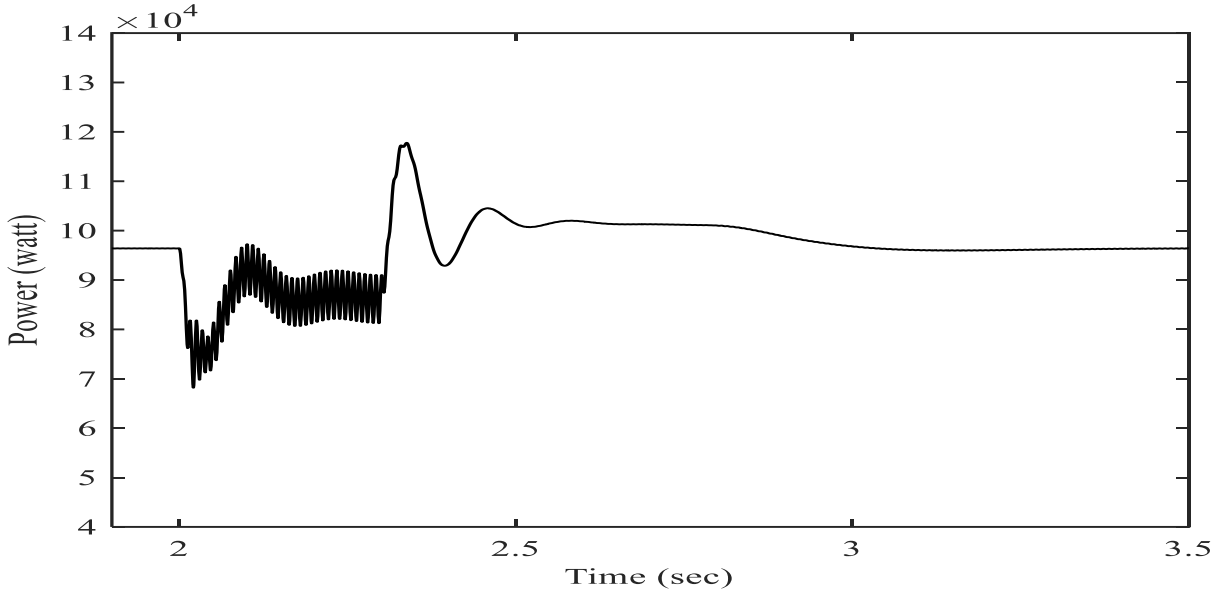

Figure 1.28 Pout having double-fundamental frequency oscillations during a-g fault in conventional positive sequence synchronous reference frame controller

In conventional positive sequence synchronous reference frame controllers double-fundamental frequency oscillations appear in output power. For instance, Figure 1.28 shows Pout having double-fundamental frequency oscillations during an a-g fault.

If dual current controller is used for the inverter, positive and negative sequence currents can be controlled simultaneously which means in (1.31), $i_d^+, i_q^+, i_d^- \; and \; i_q^-$ can be controlled. The controller may have different objectives, such as suppression of negative sequence current, suppression of active power oscillations or suppression of reactive power oscillations. The controller for suppression of active power oscillations is one of the common methods that is also implemented in this project. The active power imbalance causes double-fundamental frequency oscillations in DC voltage as $P_c, and \; P_s$ are not zero. To eliminate $P_c, and \; P_s$ the references are calculated as follows [14][15]:

$$\begin{bmatrix} i_d^{+*} \\ i_q^{+*} \\ i_d^{-*} \\ i_q^{-*} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} v_d^+ & v_q^+ & v_d^- & v_q^- \\ v_q^+ & -v_d^+ & v_q^- & -v_d^- \\ v_d^- & v_q^- & v_d^+ & v_q^+ \\ v_q^- & -v_d^- & -v_q^+ & v_d^+ \end{bmatrix}^{-1} \begin{bmatrix} P_0 \\ Q_0 \\ 0 \\ 0 \end{bmatrix} = \frac{2P_0}{3D}\begin{bmatrix} v_d^+ \\ v_q^+ \\ -v_d^- \\ -v_q^- \end{bmatrix} + \frac{2Q_0}{3F}\begin{bmatrix} v_q^+ \\ -v_d^+ \\ v_q^- \\ -v_d^- \end{bmatrix} \tag{1.32}$$

$$D = \left[(v_d^+)^2 + \left(v_q^+\right)^2\right] - \left[(v_d^-)^2 + \left(v_q^-\right)^2\right]$$

$$F = \left[(v_d^+)^2 + \left(v_q^+\right)^2\right] + \left[(v_d^-)^2 + \left(v_q^-\right)^2\right]$$

Where P_0 is determined by the PI controller of voltage of the DC capacitor.
Figure 1.29, shows the schematic of the implemented DDSRL-PLL and the dual current controller.

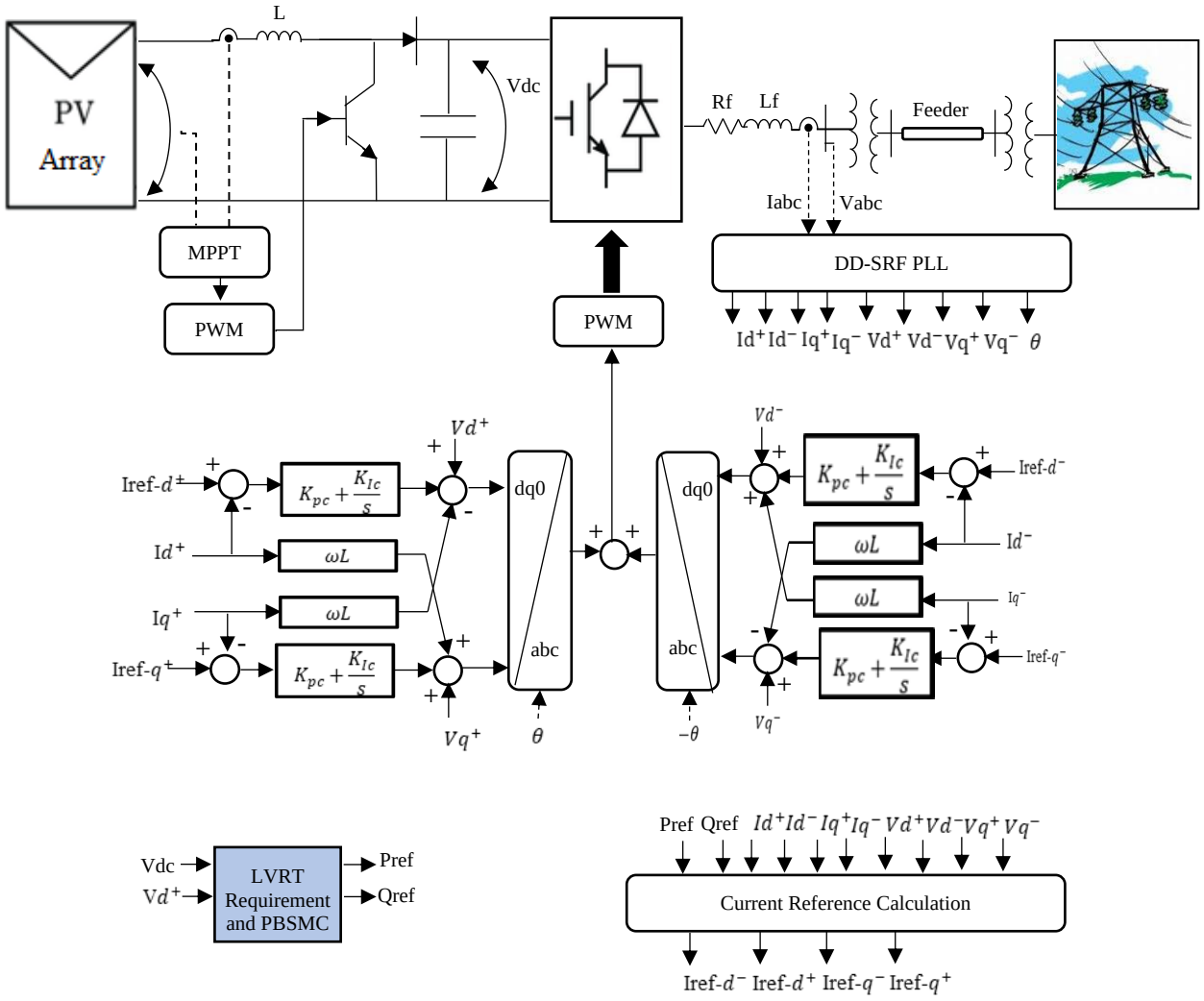

Figure 1.29 Schematic of the dual current controller for handling unbalanced faults.

1.4.1 Performance of Controllers in PV Power Plant: Unbalanced Fault Cases

To study the performance of different methods in facing unbalanced faults, different fault cases are simulated as follows.

CASE 1: A L-L-g fault (unbalanced fault) with a ground resistance of 2 ohms and a phase resistance of 2 ohms is applied. The fault occurs at 4.4 seconds and is cleared at 4.75 seconds. Figure 1.30 to Figure 1.32 show the results of different methods. As can be seen, the dual current controller eliminated double-fundamental frequency oscillations successfully. AW methods also enhance the transitioning of the inverter to the post fault condition. PBSMC method also provides similar or better results compared to other methods.

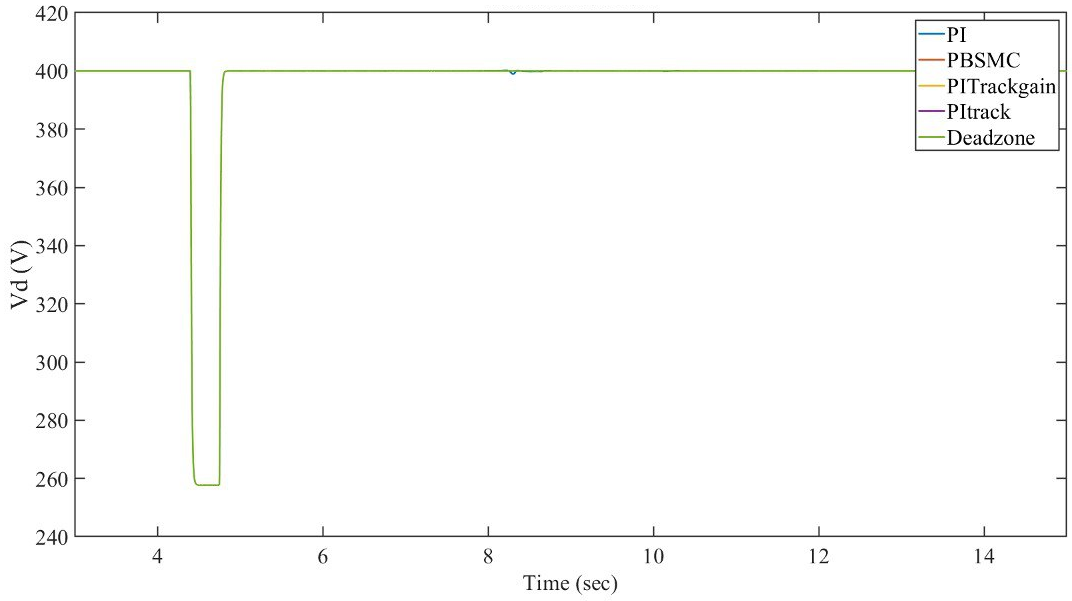

Figure 1.30 Vd in the unbalanced fault CASE 1

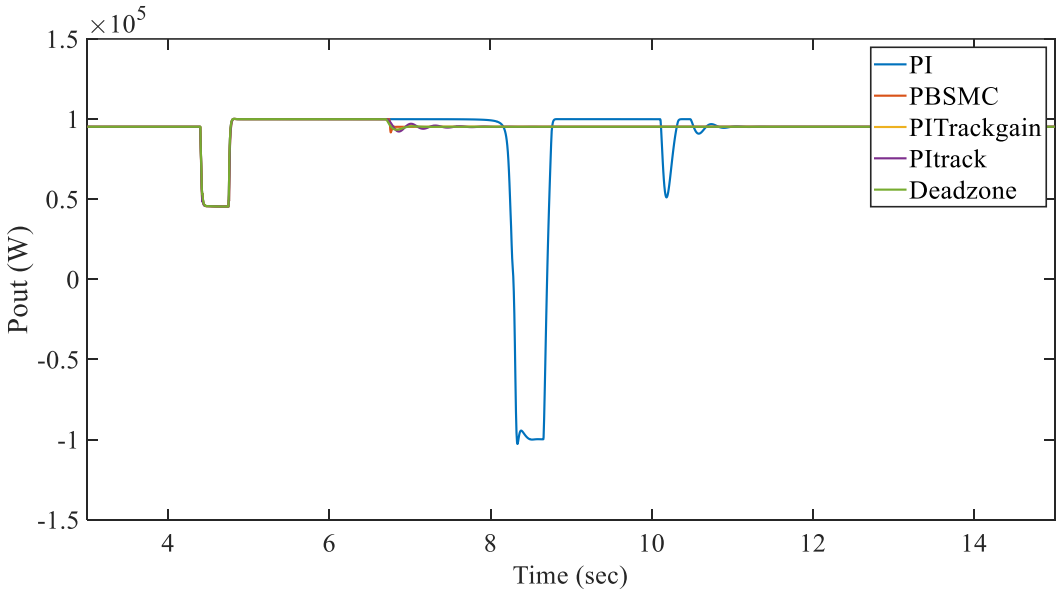

Figure 1.31 Pout for the unbalanced fault CASE 1

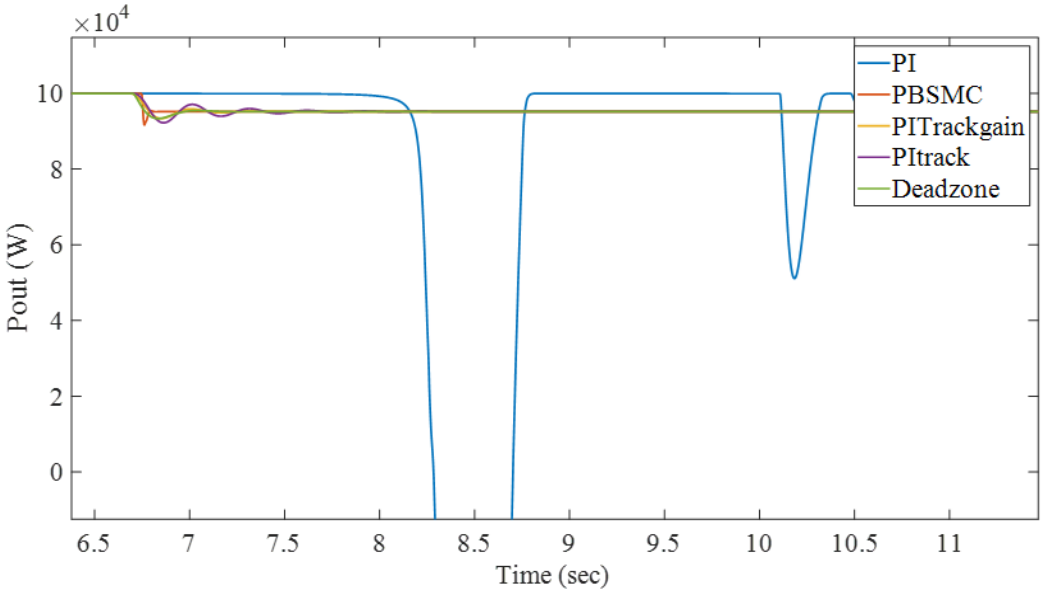

Figure 1.32 Pout zoomed on the saturation time for the unbalanced fault CASE 1

CASE 2: In this case a two-phase to ground fault is simulated that lasts for a longer duration compared to the previous case, starting at 3.4 seconds and continuing until 3.8 seconds Additionally, the ground resistance has been decreased to 2 ohms. Figure 1.33 to Figure 1.35 show the results in this case.

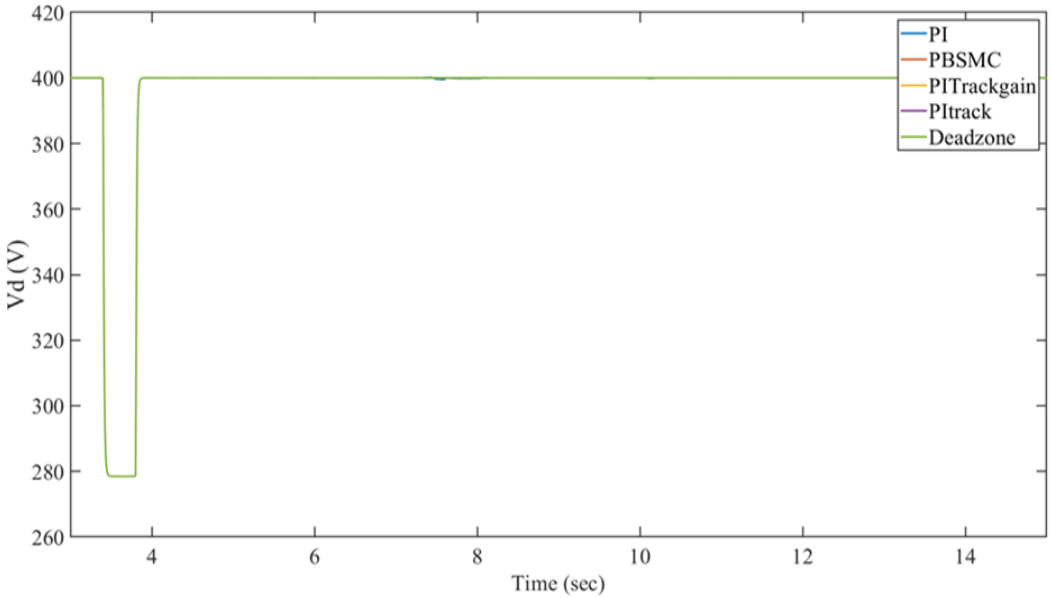

Figure 1.33 Vd in the unbalanced fault CASE 2

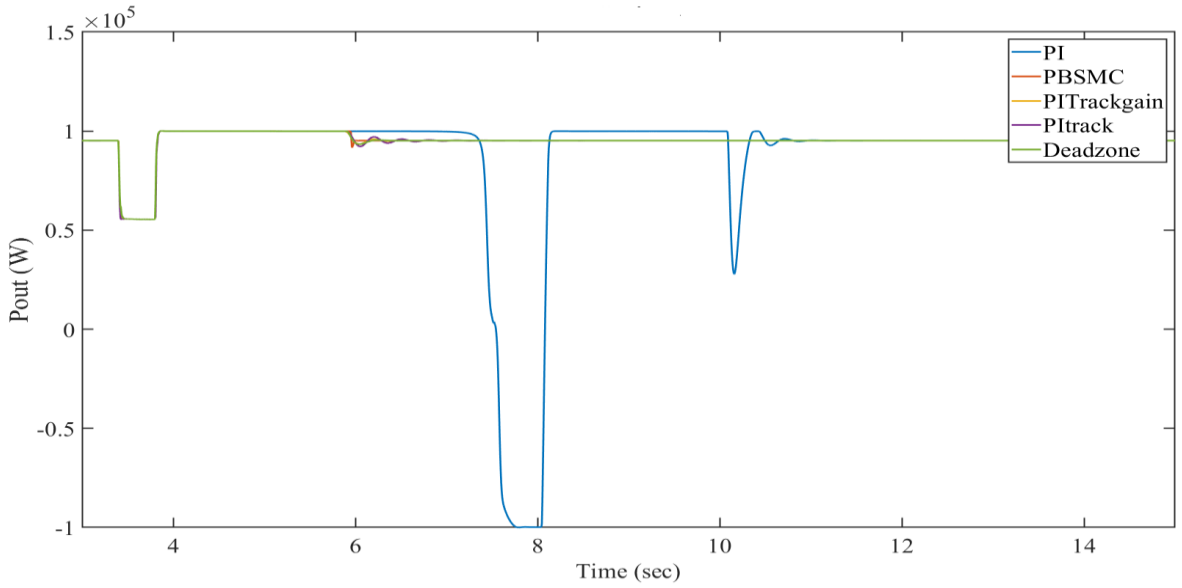

Figure 1.34 Pout in the unbalanced fault CASE 2

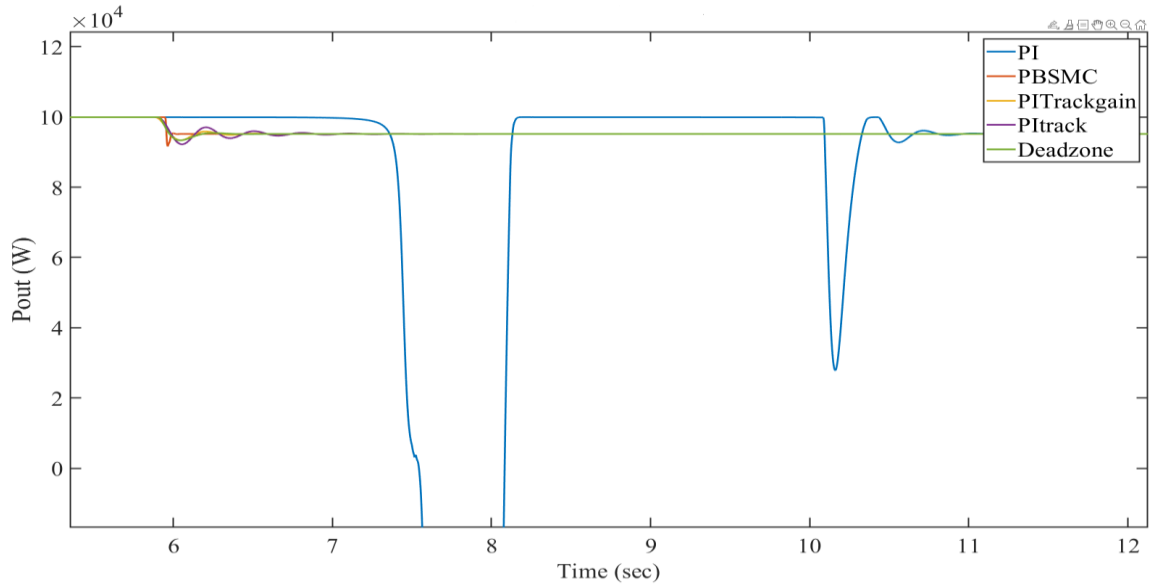

Figure 1.35 Pout zoomed on the saturation time for the unbalanced fault CASE 2

CASE 3: In this scenario, a line-to-line fault is simulated. The fault resistance is 2 ohms. The fault occurs at 4.4 sec and is cleared at 4.75 sec. Figure 1.36 to Figure 1.38 show the simulation results of different methods.

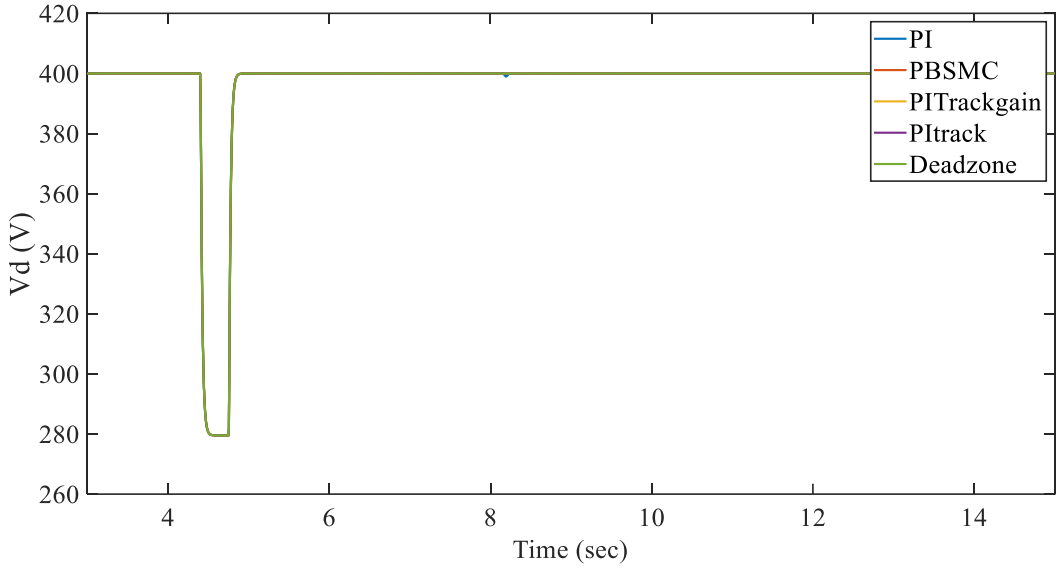

Figure 1.36 Vd in the unbalanced fault CASE 3

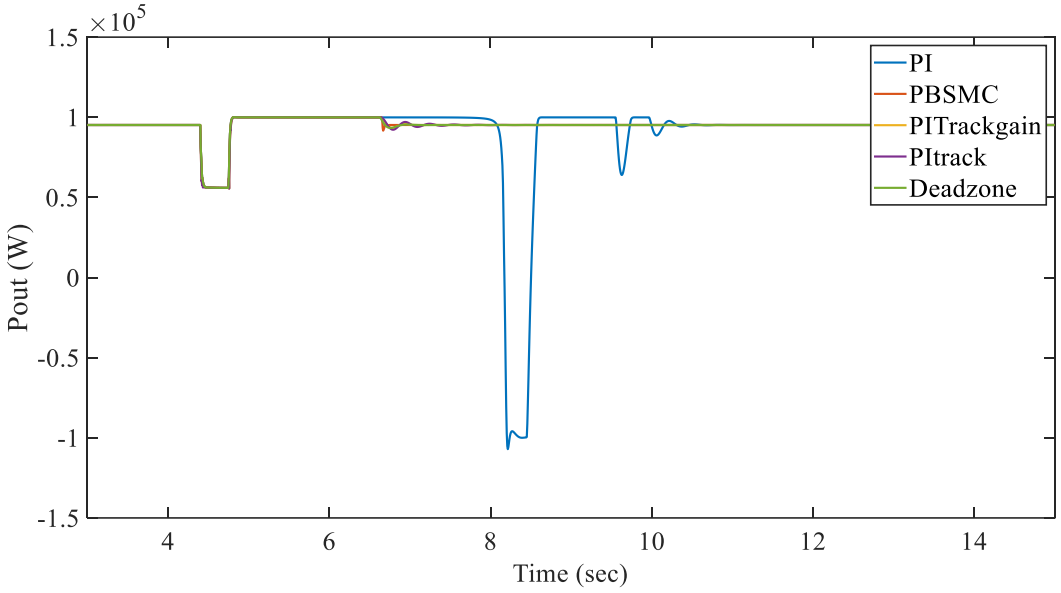

Figure 1.37 Pout in the unbalanced fault CASE 3

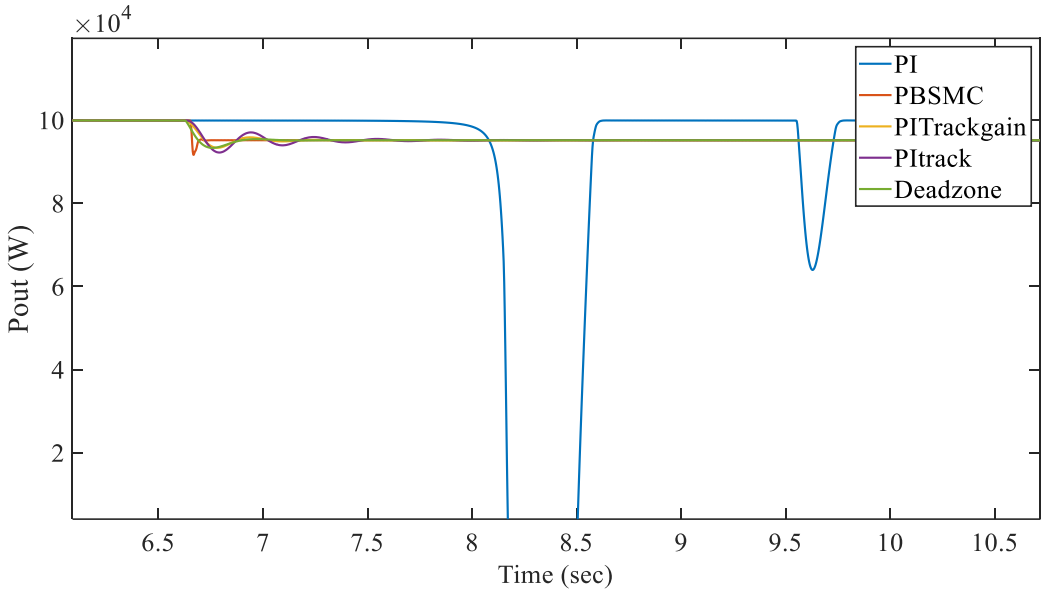

Figure 1.38 Pout zoomed on the saturation time for the unbalanced fault CASE 3

CASE 4: A line to-ground fault is considered in this case. The fault resistance is 2 ohms. The fault occurs at time 4.4 sec and is cleared at 4.75 sec. Figure 1.39 to Figure 1.41 show the simulation results. In this case also AW methods help the PI controller to have smooth transition to post-fault condition. Specifically, PBSMC has same or better performance compared to other methods.

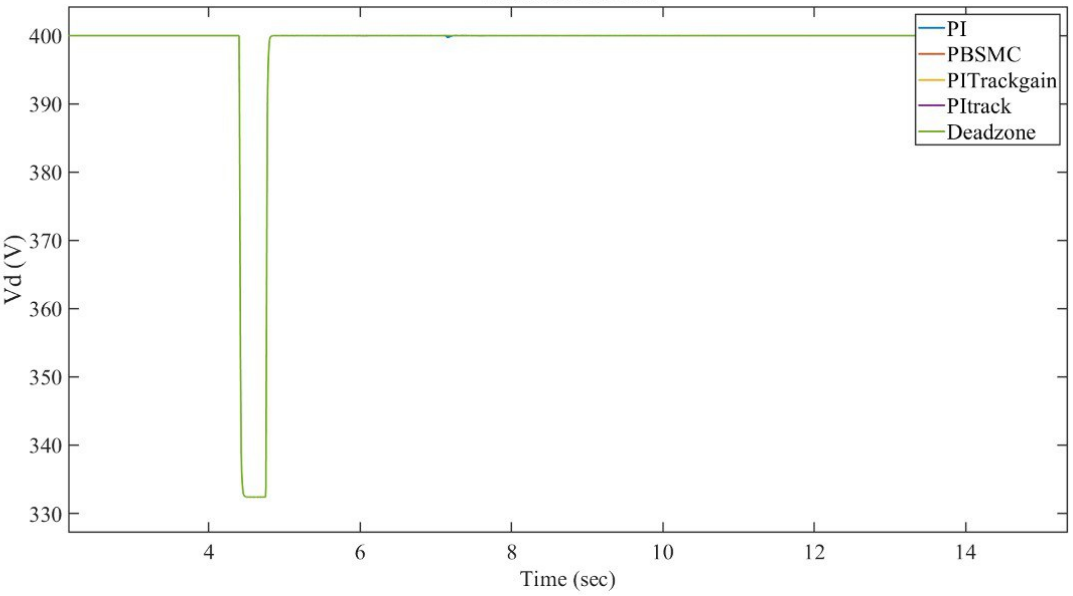

Figure 1.39 Vd in the unbalanced fault CASE 4

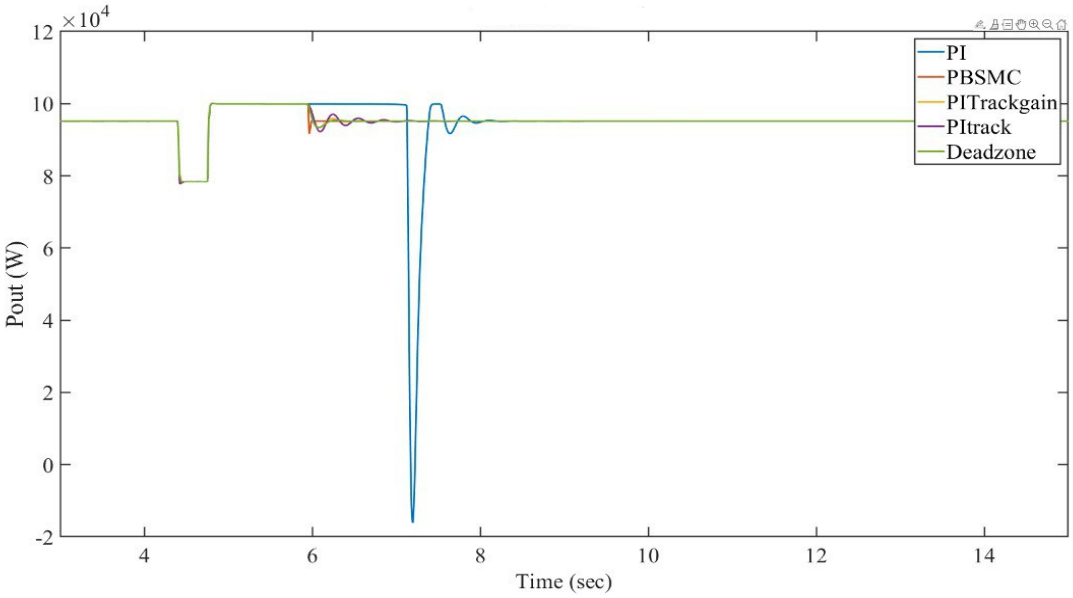

Figure 1.40 Pout in the unbalanced fault CASE 4

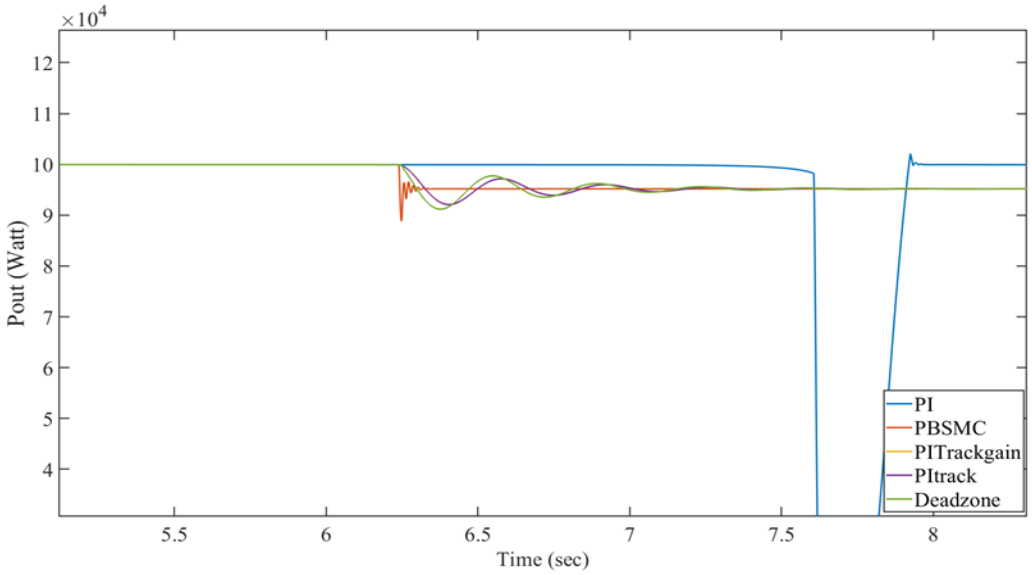

Figure 1.41 Pout zoomed on the saturation time for the unbalanced fault CASE 4

CASE 5: In this case a single phase to ground fault is simulated that lasts for a longer duration compared to previous case, starting at 3.4 seconds and continuing until 3.8 seconds. Additionally, the ground resistance is 0.2 ohms. Figure 1.42 to Figure 1.44 show the results of this case.

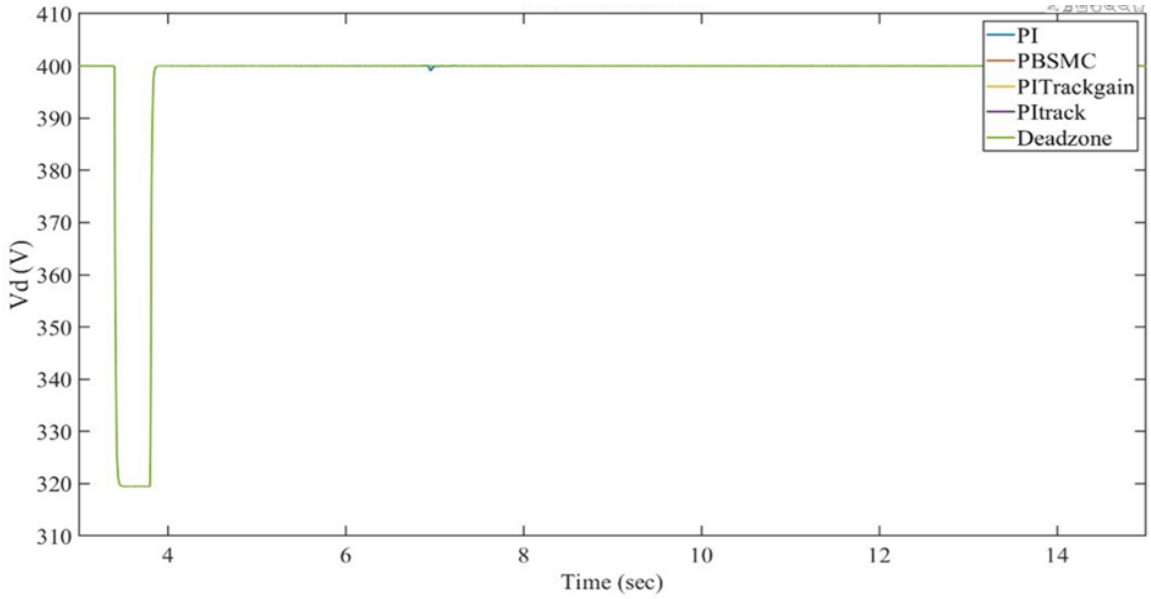

Figure 1.42 Vd in the unbalanced fault CASE 5

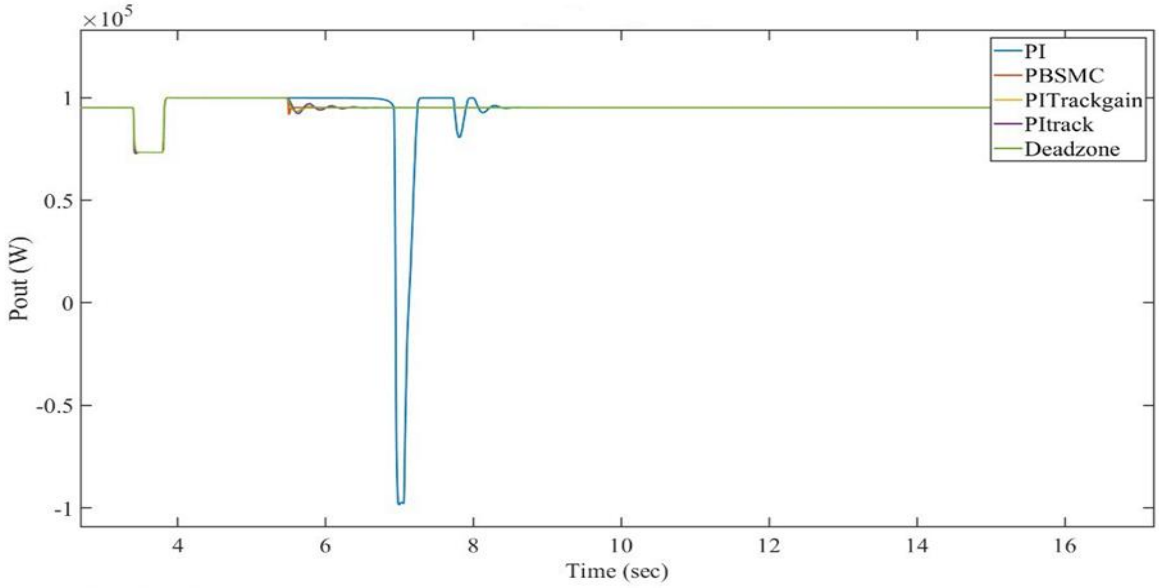

Figure 1.43 Pout in the unbalanced fault CASE 5

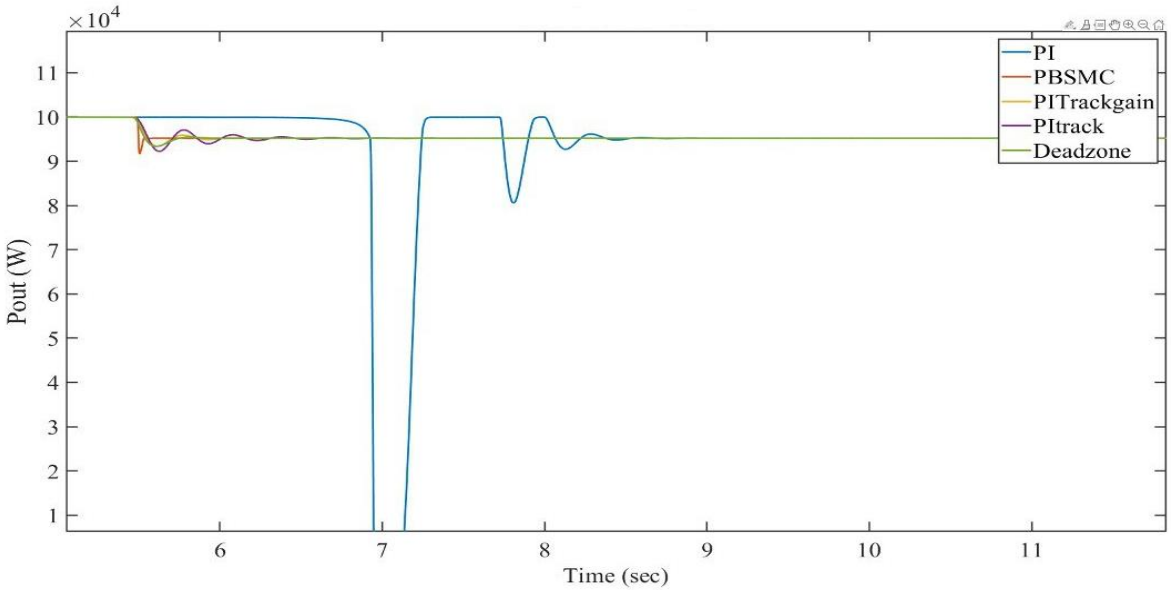

Figure 1.44 Pout zoomed on the saturation time for the unbalanced fault CASE 5

1.5 Conclusions

This project investigated the impacts of saturations of controllers due to different types of faults. Balanced and unbalanced faults, with different durations were simulated. Several anti-wide up methods were implemented. Moreover, a controller called proxy based sliding mode controller (PBSMC) was simulated. According to case study results, to enable seamless transition from during fault to post-fault condition addressing the saturation of controllers is essential. The results also showed PBSMC has similar or better results compared to several implemented anti-windup methods. Tuning AW methods is a heuristic process. In contrast, tuning the PBSMC parameter is a straightforward process which makes it suitable for practical application. The case study results showed the saturation of PI controller of the DC link voltage is influential on the outputs of inverter.

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