Partha Pratim Pande

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Education

Ph.D. (Electrical & Computer Engineering), University of British Columbia, 2005

M.S (Computer Science), National University of Singapore, 2002

Appointments

Boeing Centennial Chair in Computer Engineering	*Washington State University*	2013-
Professor, School of EECS	*Washington State University*	*2014 –*
Associate Professor, School of EECS	*Washington State University*	*2011- 2014*
Asst. Professor, School of EECS	*Washington State University*	2005- 2011

Awards

NSF CAREER Award, 2009
Anjan Bose Outstanding Researcher Award, College of Engineering and Architecture, Washington State University, 2013.
Outstanding Researcher Award, School of EECS, Washington State University, 2013.
Early Career Research Award, School of EECS, Washington State University 2012.
Best paper award nomination, International Conference on Compilers, Architectures and Synthesis of Embedded Systems, CASES 2015.

Leadership Roles in Research Community

(1) Journal Leadership:
   a. Editor-in-Chief (EIC), IEEE Transactions on Multiscale Computing Systems (TMSCS) 2015-
   b. Associate Editor-in-Chief (A-EIC), IEEE Design and Test (D&T) 2014-
   c. Chair, EIC search committee of an IEEE Transactions (exact name of the transactions can not be disclosed due to IEEE's unanimity requirement)

(2) Associate Editor:
   a. IEEE Transactions on VLSI (TVLSI) 2015-
   b. ACM Journal on Emerging Technologies in Computing Systems (JETC) 2013-
   c. Sustainable Computing – Informatics and Systems (SUSCOM) 2011-

(3) Technical Program Committee Chair:
   a. IEEE/ACM Network on Chip Symposium NOCS 2015
   b. IEEE International Green Computing Conference 2014

(4) General Chair:
   a. IEEE International Green Computing Conference, 2015
   b. IEEE/ACM Network on Chip Symposium NOCS 2016

(5) Tutorial Presenter:
   a. IEEE/ACM Network on Chip Symposium NOCS 2013
   b. Design, Automation and Test in Europe (DATE) 2014
   c. IEEE System-on-Chip Conference (SOCC) 2014

Current Research Interests: My current research principally revolves around the broad topic of Network on Chip (NoC), which has emerged as the communication backbone for multi-core chips. With my graduate students and collaborators I am working on the following projects.

- **On-chip wireless communication network:** The continuing progress and integration levels in silicon technologies make complete end-user systems on a single chip possible. This massive level of integration makes modern multi-core chips all pervasive in domains ranging from weather forecasting, astronomical data analysis, and biological applications to consumer

electronics and smart phones. NoCs have emerged as communication backbones to enable a high degree of integration in multi-core SoCs. Despite their advantages, an important performance limitation in traditional NoCs arises from planar metal interconnect-based multi-hop communications, wherein the data transfer between far-apart blocks causes high latency and power consumption. The latency, power consumption, and interconnect routing problems of NoCs can be simultaneously addressed by replacing multi-hop wired paths with high-bandwidth single-hop long-range wireless links. Our aim is to design wireless NoC architectures based on small-world graphs. Small-world graphs have a very short average path length, defined as the number of hops between any pair of nodes. The average shortest path length of small-world graphs is bounded by a polynomial in log(N), where N is the number of nodes, making them particularly interesting for efficient communication with minimal resources. NoCs incorporating small-world connectivity can perform significantly better than locally interconnected mesh-like networks, yet they require far fewer resources than a fully connected system.

- **NoC-based hardware accelerators for Biocomputing:** The gap between data generation and data processing is rapidly widening in biocomputing applications, and to close this gap it is imperative to assimilate the latest of breakthroughs in the Integrated Circuit (IC) design community into mainstream biocomputing research. Integrating huge number of processing cores on a single chip can help realize orders of magnitude improvement in performance and eventually will bridge the gap between data generation and data processing. In this project our aim is to design NoC-based hardware accelerators for different biocomputing applications, like sequence alignment and phylogenetic tree construction.
- **Sustainable Computing:** While traditional cluster computers are more constrained by power and cooling costs for solving extreme-scale (or exascale) problems, the continuing progress and integration levels in silicon technologies make possible complete end-user systems on a single chip. This massive level of integration makes modern multicore chips all pervasive in domains ranging from climate forecasting and astronomical data analysis, to consumer electronics, smart phones, and biological applications. Consequently, designing multicore chips for exascale computing while using the embedded systems design principles looks like a promising alternative to traditional cluster-based solutions. This project aims to investigate new, far-reaching design methodologies that can help breaking the energy efficiency wall in massively integrated single-chip computing platforms.
- **Machine Learning inspired Three-dimensional (3D) NoC Architectures:** Three-dimensional (3D) Network-on-Chip (NoC) is an emerging technology that has the potential to achieve high performance with low power consumption for multicore chips. However, to fully realize their potential, we need to consider novel 3D NoC architectures. In this work, inspired by the inherent advantages of small-world (SW) 2D NoCs, we explore the design space of SW network-based 3D NoC architectures. We leverage machine learning to intelligently explore the design space to optimize the placement of both planar and vertical communication links for energy efficiency.

Research Grants: (Total ~4.5 Million)

Serial No.	Title	Source	Role	Amount	Duration
(1)	CAREER: Reliable On-Chip Wireless Communication Network for Multi-Core Systems	NSF	PI	$450k	07/01/09 - 06/30/14
(2)	DC: Small: Efficient Algorithms for Data-intensive Biocomputing	NSF	Co-PI	$435k+$16k REU	06/01/09 - 07/31/13
(3)	II-NEW: Acquisition of Test and Measurement Equipment Enabling	NSF	PI	$645k	02/01/11- 02/01/14

	Design of Wireless Networks-on-Chip for Multi-Core Systems				
(4)	SHF: CSR: Medium: Collaborative Research: Hierarchical On-Chip Millimeter-Wave Wireless Micro-Networks for Multi-Core Systems	NSF	Lead PI	$800K	06/01/12-05/31/16
(5)	Millimeter-Wave Wireless Network-on-Chip Architectures for Multi-Core Systems	Army Research Office (ARO)	PI	$373K	08/16/12-12/31/15
(6)	Collaborative Research: On-chip Multi-channel Millimeter-wave Wireless Links for Multi-core Platforms	NSF	Co-PI	$490k	10/16/12-10/15/16
(7)	Equipment for research on wireless network on chip architectures for multicore systems	DURIP, ARO	PI	$249,964	8/1/13-7/31/14
(8)	REU Site: New-generation Power-efficient Computer Systems Design	NSF	Co-PI	$323,660	05/01/14-04/30/17
(9)	SHF: NeTS: Medium: Collaborative Research: The Power of Less Wiring: Wireless NoC-enabled Voltage-Frequency Islands (VFIs) for Energy-Efficient Multicore Platforms	NSF	WSU PI	$625,000	08/01/15-07/31/18
(10)	Student Travel Sponsorship for the IEEE/ACM International Symposium on Networks-on-Chip 2015	NSF	PI	$10,000	07/15/15-07/14/16

Publications: (Citation Count: 3426, H-index: 29)
(1) Journal Papers:

(a) Published/ Accepted

1. Ryan Gary Kim, Wonje Choi, Guangshuo Liu, Ehsan Mohandesi, Partha Pratim Pande, Radu Marculescu and Diana Marculescu, **"Wireless NoC for VFI-Enabled Multicore Chip Design: Performance Evaluation and Design Trade-offs",** IEEE Transactions on Computers (in press)

2. Jacob Murray, Nghia Tang, Partha Pratim Pande, Deukhyoun Heo and Behrooz Shirazi, **"DVFS Pruning for Wireless NoC Architecture",** IEEE Design and Test (in press).

3. Xinmin Yu, Hooman Rashtian, Shahriar Mirabbasi, Partha Pratim Pande and Deukhyoun Heo, **"An 18.7-Gb/s 60-GHz OOK Demodulator in 65-nm CMOS for Wireless Network-on-Chip,"** IEEE Trans. on Circuits and Systems 62-I (3): 799-806 (2015).

4. Xinmin Yu, Suman Prasad Sah, Hooman Rashtian, Shahriar Mirabbasi, Partha Pratim Pande and Deukhyoun Heo, **"A 1.2-pJ/bit 16 Gb/s 60-GHz OOK Transmitter in 65-nm CMOS for Wireless Network-On-Chip,"** IEEE Transactions on Microwave Theory and Techniques, vol.62, no.10, pp.2357, 2369, Oct. 2014.

5. Paul Wettin, Ryan Kim, Jacob Murray, Xinmin Yu, Amlan Ganguly, Partha Pratim Pande and Deukhyoun Heo, **"Design Space Exploration for wireless NoCs Incorporating Irregular Network Routing",** IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 33, Issue 11, pp. 1732-1745, Nov. 2014.

6. Xinmin Yu, Joe Baylon, Paul Wettin, Deukhyoun Heo, Partha Pratim Pande and Shahriar Mirabbasi, **"Architecture and Design of Multi-Channel Millimeter-Wave Wireless Network-on-Chip",** IEEE Design and Test, Vol. 31, Issue 6, Nov/Dec 2014, pp. 19-28.

7. Jacob Murray, Ryan Kim, Paul Wettin, Partha Pratim Pande and Behrooz Shirazi, **"Performance Evaluation of Congestion-Aware Routing with DVFS on a Millimeter-Wave Small World Wireless NoC",** ACM Journal of Emerging Technologies in Computing Systems (JETC), Volume 11 Issue 2, November 2014.

8. Ipshita Datta, Debasish Datta and Partha Pratim Pande, **"Design Methodology for Optical Interconnect Topologies in NoCs with BER and Transmit Power Constraints",** IEEE/OSA Journal of Lightwave Technology, Vol. 32, Issue 1, January 2014, pp. 163-175.

9. Turbo Majumder, Partha Pratim Pande and Ananth Kalyanaraman, **"Hardware Accelerators in Computational Biology: Application, Potential and Challenges"**, IEEE Design and Test, Vol. 31, Issue 1, February 2014, pp. 8-18.

10. Jacob Murray, Teng Lu, Paul Wettin, Partha Pratim Pande and Behrooz Shirazi, **"Dual-Level DVFS-enabled Millimeter-Wave Wireless NoC Architectures",** ACM Journal of Emerging Technologies in Computing Systems (JETC), Volume 10 Issue 4, May 2014.

11. Turbo Majumder, Partha Pratim Pande and Ananth Kalyanaraman, "**Wireless NoC Platforms for Maximum Likelihood Phylogeny Reconstruction**", IEEE Design and Test (D&T), Vol. 31, Issue 3, May/June 2014, pp. 54-64.

12. Haera Chung, Christof Teuscher and Partha Pande, **"Design and Evaluation of Technology-Agnostic Heterogeneous Networks-on-Chip",** ACM Journal of Emerging Technologies in Computing Systems (JETC), Volume 10 Issue 3, April 2014.

13. Jacob Murray, Teng Lu, Partha Pratim Pande, Behrooz Shirazi, **"Sustainable DVFS-Enabled Multi-Core Architectures with On-Chip Wireless Links"** Advances in Computers 88: 125-158 (2013)

14. Turbo Majumder, Partha Pande, Ananth Kalyanaraman**, "High-Throughput, Energy-Efficient Network-on-Chip-Based Hardware Accelerators",** Sustainable Computing, Informatics and Systems (SUSCOM), Elsevier, Volume 3, Issue 1, March 2013, Pages 36–46**.**

15. Sujay Deb, Kevin Chang, Xinmin Yu, Suman Sah, Miralem Cosic, Amlan Ganguly, Partha Pratim Pande, Benjamin Belzer and Deukhyoun Heo, "**Design of an Energy Efficient**

CMOS Compatible NoC Architecture with Millimeter-Wave Wireless Interconnects", IEEE Transactions on Computers (TC), Vol.62, no.12, pp.2382-2396, Dec. 2013.

16. Paul Wettin, Amlan Ganguly, Anuroop Vidapalapati and Partha Pratim Pande, "**Complex Network Enabled Robust Wireless Network-on-Chip Architectures**", ACM Journal of Emerging Technologies in Computing Systems (JETC), Vol. 9, Issue 3, September 2013.

17. Sujay Deb, Amlan Ganguly, Partha Pratim Pande, Benjamin Belzer and Deukhyoun Heo, "**Wireless NoC as Interconnection Backbone for Multicore Chips: Promises and Challenges",** IEEE Journal on Emerging and Selected Topics in Circuits and Systems (JETCAS), Vol. 2, No.2, June 2012, pp. 228-239.

18. Turbo Majumder, Michael Borgens, Partha Pratim Pande and Ananth Kalyanraman, "**On-Chip Network-Enabled Multi-Core Platforms Targeting Maximum Likelihood Phylogeny Reconstruction**", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), Vol. 31, No.7, July 2012, pp. 1061-1073.

19. Kevin Chang, Sujay Deb, Amlan Ganguly, Xinmin Yu, Suman Prasad Sah, Partha Pratim Pande, Benjamin Belzer and Deukhyoun Heo, "**Performance Evaluation and Design Trade-Offs for Wireless Network-on-Chip Architectures**", ACM Journal on Emerging Technologies in Computing Systems, Vol. 8, No. 3, August 2012

20. Turbo Majumder, Souradip Sarkar, Partha Pratim Pande and Ananth Kalyanaraman, "**NoC-Based Hardware Accelerator for Breakpoint Phylogeny**", IEEE Transactions on Computers (TC), Vol. 61, N0. 6, June 2012, pp. 857-869.

21. Partha Pratim Pande and Sriram Vangal, **"Guest Editors' Introduction: Promises and Challenges of Novel Interconnect Technologies",** IEEE Design and Test of Computers, Volume 27, Issue 4, July/August 2010, pp. 6-9.

22. Amlan Ganguly, Kevin Chang, Sujay Deb, Partha Pratim Pande, Benjamin Belzer, Christof Teuscher, **"Scalable Hybrid Wireless Network-on-Chip Architectures for Multi-Core Systems"**, IEEE Transactions on Computers, Vol. 60, Issue 10, pp. 1485-1502.

23. Souradip Sarkar, Gaurav Ramesh Kulkarni, Partha Pratim Pande and Ananth Kalyanaraman, "**Network-on-Chip Hardware Accelerators for Biological Sequence Alignment"**, IEEE Transactions on Computers, Vol. 59, Issue 1, January 2010, pp. 29-41.

24. Amlan Ganguly, Partha Pratim Pande, Benjamin Belzer, **"Crosstalk-Aware Channel Coding Schemes for Energy Efficient and Reliable NoC Interconnects"**, IEEE Transactions on VLSI, Vol. 17, Issue 11, November 2009, pp. 1626-1639.

25. Brett S. Feero, Partha Pratim Pande, **"Networks-On-Chip in a Three Dimensional Environment: A Performance Evaluation"**, IEEE Transactions on Computers, vol.58, no. 1, January 2009, pp. 32-45.

26. Amlan Ganguly, Partha Pratim Pande, Benjamin Belzer, Cristian Grecu, **"Design of Low power & Reliable Networks on Chip through joint Crosstalk Avoidance and Multiple Error Correction Coding"**, Journal of Electronic Testing: Theory and Applications (JETTA), Special Issue on Defect and Fault Tolerance, June 2008, pp. 67-81.

27. Partha Pratim Pande**,** Amlan Ganguly, Haibo Zhu, Cristian Grecu, **"Energy Reduction through Crosstalk Avoidance Coding in Networks on Chip",** Journal of System Architecture (JSA), Vol. 54/ 3-4, March-April 2008, pp.441-451.

28. Cristian Grecu, André Ivanov, Res Saleh, Partha Pratim Pande **"Testing Network on Chip Communication Fabrics"**, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 26, No. 12, December 2007, pp. 2201-2214.

29. Resve Saleh, Steve Wilton, Shahriar Mirabbasi, Alan Hu, Mark Greenstreet, Guy Lemieux, Partha Pratim Pande, Cristian Grecu, André Ivanov **"System-on-Chip: Reuse and Integration",** Proceedings of IEEE, Volume 94, issue 6, June 2006 pp. 1050-1069.

30. Partha Pratim Pande, Cristian Grecu, André Ivanov, Res Saleh, Giovanni De Micheli "**Design, Synthesis and Test of Networks on Chip: Challenges and Solutions "**, IEEE Design and Test of Computers, Volume 22, Issue 5, Sept.-Oct. 2005 pp. 404 – 413.

31. Cristian Grecu, Partha Pratim Pande**,** André Ivanov, Res Saleh, "**Timing Analysis of Network on Chip Architectures for MP-SoC Platforms"**, Microelectronics Journal, Elsevier, Vol. 36, issue 9, pp. 833-845, August 2005.

32. Partha Pratim Pande, Cristian Grecu, Michael Jones, André Ivanov, Res Saleh, "**Performance Evaluation and Design Trade-offs for Network on Chip Interconnect Architectures***"*, IEEE Transactions on Computers, vol. 54, no. 8, pp. 1025-1040, August 2005.

(b) Under Review

33. Xian Li, Karthi Duraisamy, Turbo Majumder, Paul Bogdan and Partha Pratim Pande, **"Enabling Closed Loop Control with Networks-on-Chip",** IEEE Transactions on VLSI.

34. Ryan Gary Kim, Wonje Choi, Zhuo Chen, Partha Pratim Pande, Diana Marculescu and Radu Marculescu, **"Wireless NoC and Dynamic VFI Co-Design: Energy Efficiency without Performance Penalty",** IEEE Transactions on VLSI.

(2) Edited Book:

35. Partha Pratim Pande, Amlan Ganguly and Krishnendu Chakrabarty, **"Design Technologies for Green and Sustainable Computing Systems",** Springer.

(2) Book Chapter:

36. Partha Pratim Pande, Amlan Ganguly, Sujay Deb and Kevin Chang, **"Energy-Efficient Network-On-Chip Architectures for Multicore Systems"**, In *Handbook of Energy-Aware and Green Computing,* Ishfaq Ahmad and Sanjay Ranka (eds.), CRC press, Taylor and Francis Group

37. Partha Pratim Pande, Cristian Grecu, Amlan Ganguly, Andre Ivanov, and Resve Saleh**, "Test and Fault Tolerance of NoC Infrastructures"**, In *Networks-on-Chips: Theory and Practice*, Fayez Gebali, Haytham Elmiligi, and M.Watheq El-Kharashi (eds.), Taylor & Francis Group LLC - CRC Press.

38. Brett Feero and Partha Pratim Pande, "**Three-Dimensional Networks-on-Chip: Performance Evaluation",** In *3D-Architectures and Networks-on-Chip*, Abbas Sheibanyrad, Frédéric Pétrot, and Axel Jantsch (eds.), Morgan Kaufmann.

(3) Conference Papers:

(a) Published/Accepted

39. Sheng-En(David) Lin, Partha Pratim Pande, Dae Hyun Kim, **"Optimization of Dynamic Power Consumption in Multi-Tier Gate-Level Monolithic 3D ICs",** To appear in the

Proceedings of IEEE International Symposium on Quality Electronic Design, ISQED 2016.

40. Sourav Das, Janardhan Rao Doppa, Partha Pratim Pande and Krishnendu Chakrabarty, "**Reliability and Performance Trade-offs for 3D NoC-Enabled Multicore Chips",** To appear in the Proceedings of IEEE Design, Automation and Test in Europe, DATE 2016.

41. Sourav Das, Janardhan Rao Doppa, Dae Hyun Kim, Partha Pratim Pande and Krishnendu Chakrabarty, **"Optimizing 3D NoC Design for Energy Efficiency: A Machine Learning Approach",** Proceedings of IEEE/ACM International Conference on Computer Aided Design, ICCAD 2015.

42. Partha Pratim Pande, Ryan Gary Kim, Wonje Choi, Zhuo Chen, Diana Marculescu and Radu Marculescu, **"The (Low) Power of Less Wiring: Enabling Energy Efficiency in Many-Core Platforms Through Wireless NoC (Invited Paper)",** Proceedings of IEEE/ACM International Conference on Computer Aided Design, ICCAD 2015.

43. Karthi Duraisamy, Hao Lu, Partha Pratim Pande and Ananth Kalyanaraman, **"High Performance and Energy Efficient Wireless NoC-Enabled Multicore Architecture for Graph Analytics",** Proceedings of the International Conference on Compilers, Architectures and Synthesis of Embedded Systems, CASES 2015.

44. T. N. Nguyen, P. P. Pande, and D. Heo "**A 64 GHz 5 mW Low Phase Noise Gm-boosted Colpitts CMOS VCO with Self-switched Biasing Technique**," in Proc. IEEE MTT Intl. Microwave Symposium (IMS) 2015.

45. P. Agarwal, P. P. Pande, and D. Heo "**25.3 GHz, 4.1 mW VCO with 34.8% Tuning Range Using a Switched Substrate-Shield Inductor**," in Proc. IEEE MTT Intl. Microwave Symposium (IMS) 2015.

46. Karthi Duraisamy, Ryan Gary Kim, Wonje Choi, Guangshuo Liu, Partha Pratim Pande, Radu Marculescu and Diana Marculescu, **"Energy Efficient MapReduce with VFI-enabled multicore Platforms",** IEEE/ACM Design Automation Conference, DAC 2015.

47. Sourav Das, Dongjin Lee, Dae Hyun Kim and Partha Pratim Pande, "**Small-World Network Enabled Energy Efficient and Robust 3D NoC Architectures",** Proceedings of ACM GLSVLSI, 2015.

48. Turbo Majumder, Partha Pratim Pande and Ananth Kalyanaraman, **"On-Chip Network-Enabled Many-Core Architectures for Computational Biology Applications",** IEEE Design, Automation and Test in Europe, DATE 2015.

49. Turbo Majumder, Xian Li, Paul Bogdan and Partha Pratim Pande, **"NoC-Enabled Multicore Architectures for Stochastic Analysis of Biomolecular Reactions",** IEEE Design, Automation and Test in Europe, DATE 2015.

50. Karthi Duraisamy, Ryan Gary Kim, Partha Pratim Pande, "**Enhancing Performance of Wireless NoCs with Distributed MAC Protocols",** IEEE International Symposium on Quality Electronic Design, ISQED 2015.

51. Ryan Kim, Guangshuo Liu, Paul Wettin, Radu Marculescu, Diana Marculescu, Partha Pratim Pande, **"Energy-Efficient VFI-Partitioned Multicore Design Using Wireless NoC Architectures"**, Proceedings of the International Conference on Compilers, Architectures and Synthesis of Embedded Systems, CASES 2014.

52. Ryan Kim, Jacob Murray, Paul Wettin, Partha Pratim Pande, Behrooz Shirazi, **"An Energy-Efficient Millimeter-Wave Wireless NoC with Congestion-Aware Routing and DVFS"**, Proceedings of ACM/IEEE International Symposium on Networks-on-Chip, NOCS 2014.

53. Jacob Murray, Paul Wettin, Ryan Kim, Xinmin Yu, Partha Pratim Pande, Behrooz Shirazi, Deukhyoun Heo, **"Thermal Hotspot Reduction in mm-Wave Wireless NoC Architectures",** Proceedings of the IEEE International Symposium on Quality Electronic Design, ISQED 2014.

54. Paul Wettin, Jacob Murray, Ryan Kim, Xinmin Yu, Partha Pratim Pande and Deukhyoun Heo, **"Performance Evaluation of Wireless NoCs in Presence of Irregular Network Routing Strategies"**, Proceedings of IEEE Design, Automation and Test in Europe (DATE), 2014.

55. S. P. Sah, X. Yu, P. Agarwal, H. Rashtian, P. P. Pande, D. Heo and Shahriar Mirabbasi, **"A V-band Wide Locking Range Injection Locked CMOS VCO for Wireless Network-on-Chip Receiver "**, Proceedings of IEEE International Microwave Symposium (IMS), 2013

56. Jacob Murray, Paul Wettin, Partha Pande, Behrooz Shirazi, Nishad Nerurkar and Amlan Ganguly, **"Evaluating Effects of Thermal Management in Wireless NoC-Enabled Multicore Architectures"**, Proceedings of IEEE International Green Computing Conference (IGCC), 2013.

57. Paul Wettin, Partha Pratim Pande, Deukhyoun Heo, Benjamin Belzer, Sujay Deb and Amlan Ganguly, **"Design Space Exploration for Reliable mm-Wave Wireless NoC Architectures"**, Proceedings of IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP), 2013.

58. Turbo Majumder, Partha Pratim Pande and Ananth Kalyanaraman, **"Network-on-chip with long-range wireless links for high-throughput scientific computation"** Proceedings of IPDPS workshop on Communication Architecture for Scalable Systems (CASS*)*, 2013.

59. Paul Wettin, Jacob Murray, Partha Pratim Pande, Behrooz Shirazi and Amlan Ganguly, **"Energy-Efficient Multicore Chip Design Through Cross-Layer Approach"**, Proceedings of IEEE Design, Automation and Test in Europe (DATE), 2013.

60. Jacob Murray, Rajath Hegde, Teng Lu, Partha Pratim Pande and Behrooz Shirazi, **"Sustainable Dual-Level DVFS-enabled NoC with on-chip Wireless Links"**, Proceedings of the IEEE International Symposium on Quality Electronic Design, ISQED 2013.

61. Jacob Murray, Partha Pratim Pande and Behrooz Shirazi, **"DVFS-Enabled Sustainable Wireless NoC Architecture"**, Proceedings of IEEE International System-on-Chip Conference (SOCC), September 2012.

62. Sujay Deb, Kevin Chang, Miralem Cosic, Amlan Ganguly, Partha Pande, Deukhyoun Heo and Benjamin Belzer, **"CMOS Compatible Many-Core NoC Architectures with Multi-Channel Millimeter-Wave Wireless Links"**, Proceedings of ACM Great Lake Symposium on VLSI, GLSVLSI 2012.

63. Jacob Murray, John Klingner, Partha Pande and Behrooz Shirazi, **"Sustainable Multi-Core Architecture with on-chip Wireless Links"**, Proceedings of ACM Great Lake Symposium on VLSI, GLSVLSI 2012.

64. Sujay Deb, Kevin Chang, Amlan Ganguly, Xinmin Yu, Christof Teuscher, Partha Pande, Deuk Heo and Benjamin Belzer, "**Design of an Efficient NoC Architecture using Millimeter-Wave Wireless Links**", Proceedings of the IEEE International Symposium on Quality Electronic Design, ISQED 2012.

65. Ipshita Datta, Debasish Datta and Partha Pratim Pande, "**BER-based Power Budget Evaluation for Optical Interconnect Topologies in NoCs"**, Proceedings of the IEEE International Symposium on Circuits and Systems, ISCAS 2012.

66. Turbo Majumder, Partha Pratim Pande and Ananth Kalyanaraman, **"Accelerating Maximum Likelihood based Phylogenetic Kernels using Network-on-Chip",** Proceedings of 23rd International Symposium on Computer Architecture and High Performance Computing - SBAC-PAD 2011.

67. Amlan Ganguly, Partha Pratim Pande, Benjamin Belzer and Alireza Nojeh, "**A Unified Error Control Scheme to Enhance the Reliability of a Hybrid Wireless Network-on-Chip"**, Proceedings of IEEE International Symposium on Defect and fault Tolerance in VLSI and Nanotechnology systems, DFTS 2011.

68. Xinmin Yu, Suman Prasad Sah, Sujay Deb, Partha Pratim Pande, Benjamin Belzer and Deukhyoun Heo, "**A Wideband Body-Enabled Millimeter-Wave Transceiver for Wireless Network-on-Chip**'', Proceedings of IEEE Midwest Symposium on Circuits and Systems, MWSCAS 2011.

69. Amlan Ganguly, Paul Wettin, Kevin Chang and Partha Pratim Pande, **"Complex Network Inspired Fault-Tolerant NoC architectures with Wireless Links"**, Proceedings of the ACM/IEEE International Symposium on Networks-on-Chip, NOCS 2011.

70. Partha Pande, Fabien Clermidy, Diego Puschini, Imen Mansouri, Paul Bogdan, Radu Marculescu and Amlan Ganguly, **"Sustainability through Massively Integrated Computing: Are We Ready to Break the Energy Efficiency Wall for Single-Chip Platforms?"** Proceedings of IEEE Design, Automation and Test in Europe (DATE) 2011.

71. Radu Marculescu, Christof Teuscher and Partha Pande, **"Unconventional fabrics, architectures, and models for future multi-core systems"**, Proceedings of CODES+ISSS 2010.

72. Sujay Deb, Kevin Chang, Amlan Ganguly and Partha Pande, **"Comparative Performance Evaluation of Wireless and Optical NoC Architectures",** Proceedings of IEEE International SOC Conference (SOCC), 27th-29th September 2010.

73. Turbo Majumder, Souradip Sarkar, Partha Pratim Pande and Ananth Kalyanaraman, "**An Optimized NoC Architecture for Accelerating TSP Kernels in Breakpoint Median Problem",** Proceedings of IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP 2010), 7th – 9th July 2010.

74. Sujay Deb, Amlan Ganguly, Kevin Chang, Partha Pratim Pande, Benjamin Belzer and Deuk Heo, **"Enhancing Performance of Network-on-Chip Architectures with Millimeter-Wave Wireless Interconnects",** Proceedings of IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP 2010), 7th -9th July, 2010

75. Souradip Sarkar, Turbo Majumder, Ananth Kalyanaraman, Partha Pratim Pande, **"Hardware Accelerators for Biocomputing: A Survey"**, Proceedings of IEEE International Symposium on Circuits and Systems, ISCAS 2010, 30th May – 2nd June, 2010.

76. Partha Pratim Pande, Amlan Ganguly, Kevin Chang, Christof Teuscher, **"Hybrid Wireless Network-on-Chip: A New Paradigm in Multi-Core Design"**, Proceedings of International Workshop on Network-on-Chip Architectures (NoCArc), December 12, 2009.

77. Luca P. Carloni, Partha Pande and Yuan Xie, **"Networks-on-Chip in Emerging Interconnect Paradigms: Advantages and Challenges",** Proceedings of the IEEE International Symposium on Networks-On-Chip, 10-13 May 2009.

78. Amlan Ganguly, Kevin Chang, Partha Pratim Pande, Benjamin Belzer and Alireza Nojeh, **"Performance Evaluation of Wireless Networks on Chip Architectures",** Proceedings of the IEEE International Symposium on Quality Electronic Design (ISQED), 16th-18th March 2009.

79. Cristian Grecu, Andre Ivanov, Resve Saleh, Claudia Rusu, Lorena Anghel, Partha Pratim Pande, Vasile Nuca, "**A flexible network-on-chip simulator for early design space exploration",** Proceedings of IEEE Microsystems and Nanoelectronics Research Conference, MNRC, October 2008.

80. Alireza Nojeh, Partha Pratim Pande, Amlan Ganguly, Samad Sheikhaei, Benjamin Belzer and Andre Ivanov, **"Reliability of wireless on-chip interconnects based on carbon nanotube antennas"**, Proceedings of IEEE International Mixed-Signals, Sensors, and Systems Test Workshop (IMS3TW) June 2008.

81. Partha Pratim Pande, Amlan Ganguly, Benjamin Belzer, Alireza Nojeh, Andre Ivanov, **"Novel Interconnect Infrastructures for Massive Multicore Chips – An Overview"**, Proceedings of IEEE International Symposium on Circuits and Systems, ISCAS 2008, 18th-21st May, 2008.

82. Jabulani Nyathi, Souradip Sarkar, Partha Pratim Pande, **"Multiple Clock Domain Synchronization for Network on Chip Architectures",** Proceedings of IEEE International SoC Conference, SOCC 2007, 26th-29th September 2007.

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101. Partha Pratim Pande, Cristian Grecu, André Ivanov, Res Saleh, **"High-Throughput Switch-Based Interconnect for Future SoCs"**, Proceedings of IEEE International Workshop on SoC for Real Time Applications, 2003, Calgary, Canada.

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Synergistic Activities:

1. NSF Panelist, CISE CCF, CPS
2. Guest Editor, IEEE Design and Test of Computers, Special Issue on Emerging Interconnect Technologies for Gigascale Integration.
3. Guest Editor, IEEE Design and Test of Computers, Special Issue on Hardware Acceleration in Computational Biology.
4. Guest Editor, ACM Journal on Emerging Technologies in Computing Systems, Special Issue on Sustainable and Green Computing Systems.
5. Keynote Speaker, NocArc 2013.
6. Presenter in special session on Wireless NoC, NOCS 2014
7. Program Committee member of the following conferences

    - IEEE Design, Automation conference, DAC 2014, 2015
    - International Conference on Hardware/Software Codesign and System Synthesis, CODES+ISSS (2013-2015).
    - IEEE/ACM International Conference on Computer-Aided Design, ICCAD 2014, 2015.
    - IEEE International Midwest Symposium on Circuits and Systems, MWSCAS, 2007 (Co-chair for the Test and Characterization track)
    - IEEE International Midwest Symposium on Circuits and Systems, MWSCAS, 2010, Publication Chair.
    - IEEE International online testing symposium, IOLTS (2007-2010)
    - Asian Test Symposium, ATS (2007, 2008)
    - IEEE International Workshop on Electronic Design, Test and Applications, DELTA (2008-2010)
    - IEEE International Symposium on Networks-on-Chip (NOCS 2009-2012, 2014)
    - IEEE Green Computing Conference (IGCC) 2013

8. Presenter in the special session on Emerging Interconnect technologies, NOCS 2013.

9. Organizer of the Hot Topic session "*Fault Tolerant Nanoscale Architectures – the Challenges and Emerging Solutions"* 25th IEEE VLSI Test Symposium, VTS 07

10. Presenter in the Hot Topic Session, *"Signal Integrity: How Can it be Designed into Multiprocessor Platforms, Systems on-Chip, and Systems in-Package?"* 24th IEEE VLSI Test Symposium, VTS 06

11. Special session organizer and session chair, IEEE International Symposium on Circuits and Systems, ISCAS 2008, 2010.

12. Workshop organizer, IEEE International Green computing Conference.

13. Special session Chair, IEEE International Symposium on Networks-on-Chip NOCS 2011.

14. Member, Computer Engineering Curriculum Committee, School of EECS, Washington State University.

15. Member, Scholarship Committee, School of EECS, Washington State University.

16. Participant of Provost's Faculty Leadership Academy (PFLA) program.

17. Reviewer for conferences like Design Automation & Test in Europe (DATE), International Conference on Computer Aided Design (ICCAD), Design Automation Conference (DAC), VLSI Test Symposium (VTS), International Test Conference (ITC), International Symposium on Circuits and Systems (ISCAS) and journals like IEEE Transaction on VLSI, IEEE Design and Test, IEEE Transactions on computer-aided design of Integrated Circuits and Systems.

Graduate Students Supervision:

(a) Current Graduate Students:

1. Ryan Kim (PhD)
2. Teng Lu (PhD), Co-advising with Behrooz Shirazi
3. Shervin Hajiamini (PhD), Co-advising with Behrooz Shirazi
4. Xian Li (PhD)
5. Dongjin Lee (PhD)
6. Wonje Choi (PhD)
7. Karthi Duraisamy (PhD)
8. Sourav Das (PhD)
9. Sheng-En Lin (PhD), Co-advising with Dae Hyun Kim

(b) Graduated:

- Paul Wettin (PhD, May 2014, currently employed at Marvell Technology)
- Jacob Murray (PhD, May 2014, currently employed as Clinical Asst. Professor Electrical Engineering, WSU at Everett Community College program)
- Turbo Majumder (PhD, May 2013, currently at Intel Labs)
- Sujay Deb (PhD, May 2012, currently Asst. Professor, Indraprastha Institute of Information Technology (IIIT), Delhi, India)
- Kevin Chang (PhD, May 2012, currently employed at ARM)
- Amlan Ganguly (PhD, August 2010, currently Asst. Professor, Rochester Institute of Technology)
- Souradip Sarkar (PhD, December 2010, currently R&D Engineer, Bell Labs)

- Haibo Zhu (MS, July 2007, currently employed at LINK_A_Media Devices, San Jose, USA)
- Brett Feero (MS, May 2008, currently employed at Apple)
- Divya Krishnan (MS, August 2010, currently working at Micron, Boise)
- Chien Chuan Hung (MS, currently working at Nvidia)

(c) Committee Member:

- Syryanarayana Tatapudi (PhD, Graduated, May 2006)
- Daniel R. Blum (PhD, Graduated, May 2007)
- Ray Robert Rydberg III (PhD, Graduated, May 2009)
- Billy J Hamon (MS, Graduated, December 2008)
- Nancy Shah (MS, Graduated, January 2009)
- Jeremy Asmussen (MS, Graduated, December 2009)
- Alex O. Mikul (MS, Graduated, December 2009)
- Gaurav Ramesh Kulkarni (MS, Graduated, December 2009)
- Thanigainathan Manivannan (MS, Graduated, December 2011)
- Philip Munson (MS, Graduated, December 2011)
- Florian Grigoleit (MS, Graduated, December 2011)
- Rajath Hegde (MS, Graduated, August 2012)
- Yu You (PhD, current)
- Huan Peng (PhD, current)
- Siqi Zhu (PhD, current)
- Xinmin Yu (PhD, current)
- Suman Prasad Sah (PhD, current)
- Pawan Agarwal (PhD, current)
- Joe Baylon (PhD, current)

Teaching Activities:

- EE 434 (ASIC and Digital Systems)
- EE 587 (System on Chip Design and Test)
- EE 586 (VLSI Design)
- EE 466 (VLSI Design)

References:

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