10.8 A 4-Element 500MHz-Modulated-BW 40mW 6b 1GS/s Analog-Time-to-Digital-Converter-Enabled Spatial Signal Processor in 65nm CMOS

Erfan Ghaderi, Chase Puglisi, Shrestha Bansal, Subhanshu Gupta

Washington State University, Pullman, WA

Next-generation phased-array systems with large modulated bandwidths (BW) and high energy efficiency will enable Gb/s wireless communications. The spatial signal processing at this large scale using state-of-the-art phase-shifter (PS)-based arrays causes unsolved challenges in dense interference-limited networks with large modulated BWs. In addition, the need for frequency-independent array gain demands low-complexity and energy/area-efficient true-time-delay(TTD)-based spatial signal processing. Recent works have demonstrated beam-nulling [1,2] and beamforming [2-4] for PS and TTD systems. In [1], a baseband(BB)-to-RF impedance translation is used for beam nulling with a swept single tone only. In [2], an autonomous spatial filter without external controls is implemented for large modulated BW. However, its PS-based method introduces frequency-dependent filtering for applications at lower RF carrier frequencies (large fractional BWs). To avoid beam-squint in beamforming, the digital TTD-based beamformer is implemented in [3] with 100MHz BW; however, the required 16 ADCs (1/element) increases the overall RX power consumption. In [4], a 100MHz analog BB beamforming architecture implementing TTD in the clock path is shown. However, the switched-capacitor implementation is insufficient to support large modulated BWs with high energy efficiency for next-generation communication links.

We present an *N*-element BB time-domain spatial signal processor (SSP) for large modulated BW multi-antenna RXs (Fig. 10.8.1). The implemented architecture is capable of three spatial signal processing modes: (1) beamforming by constructive signal combination; (2) beam-nulling by destructive signal combination; and (3) simultaneous spatial filtering of $\log_2 N$ independent interferences by non-uniform TTD extracted by Kronecker decomposition (fragmenting the input time-delay vector into $\log_2 N$ sub-vectors before filtering) [5]. In this architecture, the antenna's received signals (S_1, …, S_N) are phase-shifted, downconverted, filtered, and then applied to the BB time-domain SSP. Similar to [4], TTD is implemented through BB delay-compensating. However, the stringent design requirements of the operational amplifier used in the switched-capacitor array in [4] motivated us to implement the signal combination in the time domain through cascaded voltage-to-time converters (VTCs). The spatially processed time-domain outcome is then applied to a pipeline time-to-digital converter (TDC) for digitization and further processing (Fig. 10.8.1). The time-domain SSP benefits from digital-friendly implementation, therefore also benefiting from technology-scaling.

The detailed implementation of the time-domain SSP for a 4-element 500MHz BB RX array is presented in Fig. 10.8.2. In this 4-element array, 8 unique combinations can be implemented simply by changing the applied BB signal ($IN_{1..4}$) polarity, leveraging the differential implementation. One level of time-interleaving is employed as proof-of-concept to allow one sampling-clock-period delay compensation between the signals (1ns for a Nyquist rate sampling of 1GS/s). To compensate larger delays, a higher level of interleaving can be used [4]. In this processor, eight VTCs sample the BB signals on the sampling capacitors (C_S) with different sampling clocks (φ_{11}-φ_{42}, Fig. 10.8.2) for delay-compensation. The sampling capacitors in the first input's VTCs (VTC_{11}, VTC_{12}) are then discharged with a constant current (I_{DC}) in the σ_1 and σ_2 phases. Depending on the sampled values, two pairs of time-interleaved clocks are generated, containing the time-domain information in the first input. By applying these clocks to the discharging clocks of the sampling capacitor of the second pair of VTCs (VTC_{21}, VTC_{22}), the time-domain information of the second input is added to the first one. Continuing this trend for the remaining VTC pairs, all the input signals are added in the time domain at the output of the last pair of VTCs (VTC_{41}, VTC_{42}). The last time-interleaved clocks are then combined through OR gates to generate the non-interleaved 1GS/s time-domain information (ST_{SSP}, SP_{SSP}). The clocking phases are generated on-chip through tunable delay lines and time-interleavers.

The presented 6bit pipeline TDC (Fig. 10.8.2) consists of four residue stages and a 2bit flash TDC. At each residue stage, two raw bits of the time-domain signal are extracted, and the residue value is passed to the next stage after 2× amplification by a calibrated time amplifier (TA). The residue stage compares delayed versions of the input signals (ST_{IN}, SP_{IN}) through a NAND-based arbiter. Based on the arbiter outputs, the LOGIC unit determines the digital raw data (B_1B_0), generates a VALID pulse as an asynchronous clock for the digital-error-correction (DEC) data alignment, and selects delayed versions of the input signals as the residue clocks (ST_{OUT}, SP_{OUT}).

The pipeline TDC performance is conventionally limited by the TA linearity. In this work, a hybrid combination of TAs with companding and expanding characteristics (Fig. 10.8.2) is presented which improves the TA linearity. Independent design knobs (CAL_C, CAL_D) are added to linearize the TA. Particle Swarm Optimization (PSO) [6] is used for one-time optimization of the multiple design knobs for all the TAs simultaneously. The PSO achieves global minima by spreading out multiple particles randomly, each particle representing a possible solution. After each iteration, all the particles collaboratively arrive to the best possible solution.

The 4-element SSP is prototyped in 65nm CMOS occupying an area of 0.82mm^2 (Fig. 10.8.7). The input signals are applied through four 14bit 3.9GHz DACs on the Xilinx ZCU111 FPGA. Both the CW and wideband modulated signals are first generated in MATLAB and then uploaded on the FPGA. The time delay between the inputs, caused by the antenna spacing, is mimicked in these measurements during signal generation. The SSP delay-compensation is controlled externally by the TI DAC81416EVM. The SSP digital output is read at lower speed (40MHz) and the original data is reconstructed later by the Equivalent-Time-Sampling (ETS) technique in MATLAB.

Figure 10.8.3 shows the SSP performance for CW inputs. In the beamforming mode, a relatively constant voltage gain of 12dB is shown over the entire 500MHz BW for three different angle-of-arrivals (AoAs). The measured beam patterns of the SSP show immunity to beam-squint. In the single-interference beam-nulling mode, >40dB spatial rejection over the entire 500MHz BW is measured for three different AoAs with the corresponding beam patterns. In the two-independent-interference-filtering mode, two different scenarios are measured. For both the independent interferences >34dB spatial rejection is realized. Corresponding beam patterns are also presented. Figure 10.8.4 presents the measured spectral performance for large modulated BWs. Approximately 12dB frequency-uniform beam-forming voltage gain, ~24dB beam-nulling, and >21dB two-independent-interference filtering are demonstrated with the input voltage to the SSP set to $1V_{P\text{-}P,diff}$. The modulated BWs are chosen to visually represent the SSP results.

The constellation and EVM for the three SSP modes with a 250Mb/s 16-QAM signal are measured and presented in Fig. 10.8.5. In the beamforming mode, a 12dB stronger CW interference is added resulting in 5.0% EVM_{rms}. In the beam-nulling mode, a 12dB stronger 160MHz interference is added and 5.3% EVM_{rms} is measured. In the two-independent-interference-filtering mode, two 80MHz interferences, each 6dB stronger than the original signal, are added resulting in 9.0% EVM_{rms}. Figure 10.8.5 also shows the optimization results after applying PSO to the SSP, with 12 iterations for 400 particles. The PSO incurs minimal power overhead since it is executed offline only one time. The measured SSP power spectral density before calibration (all the TA CAL controls are VDD) and after PSO (finding the best values for TA controls) are demonstrated with 6.4dB performance improvement.

In summary, Fig. 10.8.6 compares the TTD-based SSP leveraging PSO with the prior state-of-the-art. Time-domain implementation leverages technology scalability and achieves high energy efficiency for large modulated BW.

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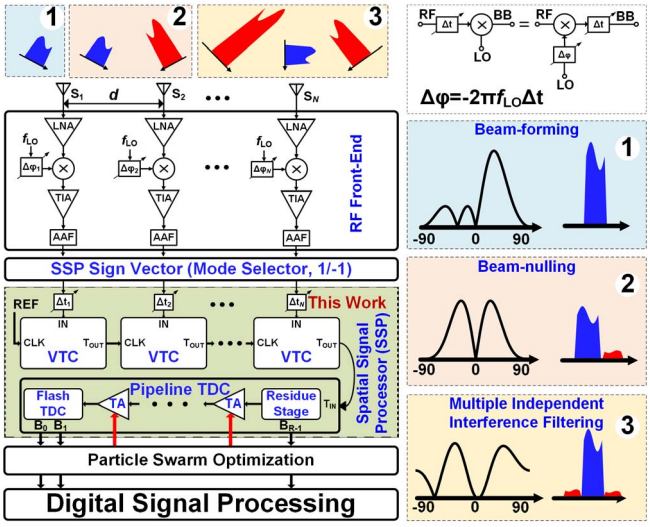

Figure 10.8.1: System architecture of the *N*-element time-domain TTD spatial signal processor (SSP) (left); three spatial processing modes (right).

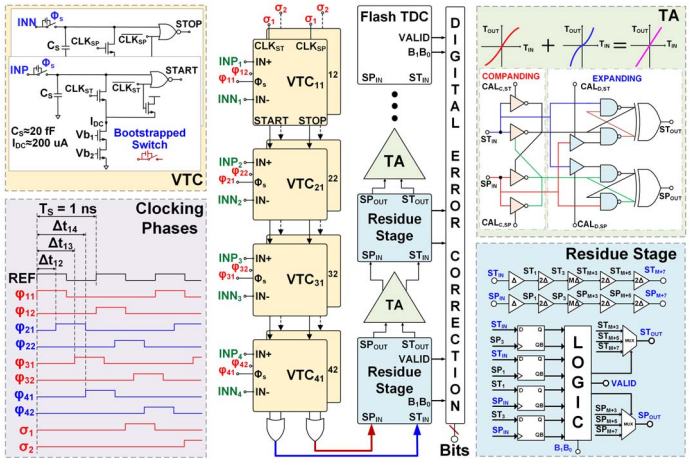

Figure 10.8.2: Circuit realization of the 4-element SSP (center); including the voltage-to-time converter (VTC, top left); time-amplifier (TA, top right); clocking phases (bottom left); and residue stage (bottom right).

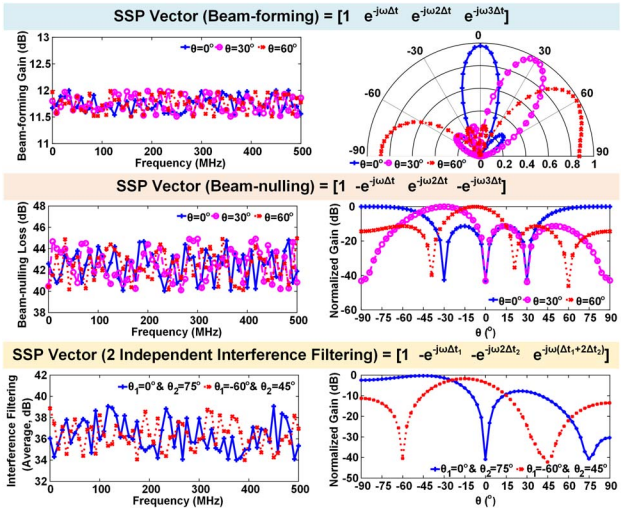

Figure 10.8.3: Measurement results of the 4-element SSP in three different spatial processing modes for swept continuous wave (CW) tone across 500MHz BW and angle-of-arrival (θ).

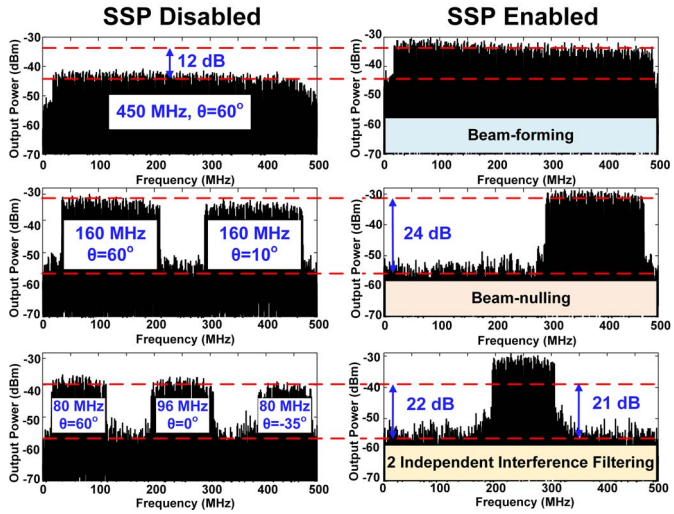

Figure 10.8.4: Measured spectral response of the 4-element SSP in three spatial processing modes for large modulated BW and different angle-of-arrival (θ). BWs are chosen for visual representation.

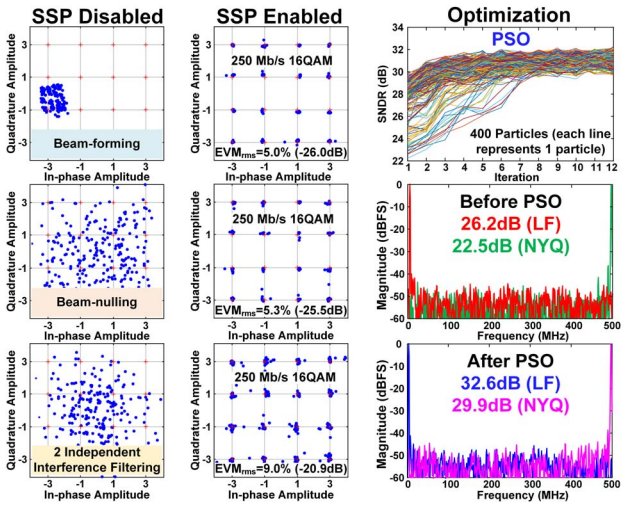

Figure 10.8.5: Measured EVM of the 4-element SSP in three spatial processing modes (speed/modulation equipment-limited) (left, center); SNDR improvement using particle swarm optimization (offline one-time) (right).

		[1] ISSCC 2017	[2] ISSCC 2019	[3] JSSC 2019	[4] TCAS-I 2019	This Work
Architecture		Phased-shift array	Phased-shift array	Digital TTD array	TTD array	**TTD array**
Functionality		Arbitrary Spatial Filtering	Beamformer + Multi-Blocker Rejection	Beamformer + ADC	Beamformer	**Beamformer + Multi-Blocker Rejection + ADC**
Domain		Voltage	Voltage	Voltage	Charge	**Time**
Technology		65nm CMOS	45nm SOI	40nm CMOS	65nm CMOS	**65nm CMOS**
Supply (V)		1.2	NR	NR	1.0	**1.0**
# Elements (*N*)		4	4	16	4	**4**
Rejection (dB)	Single-Tone	51-56	50-62	47	NA	**40-46**
	Modulated BW	NR	~20[1]	NA	NA	**24**
Rejection Mod. BW (MHz)		CW	500[2]	NA	NA	**500**
Beamforming Mod. BW (MHz)		NR	500[2]	100	100	**500**
TTD Range (ns)		NA	NA	7.5	15	**1**
Fractional BW (Mod. BW /RF Carrier Frequency)		NR	1.8% (0.5GHz/28GHz)	10.0% (0.1GHz/1GHz)	100.0% (0.1GHz/0.1GHz)[3]	**33.3% (0.5GHz/1.5GHz)[3]**
Linearity	P_{1dB} (dBm)	NR	-27.3 (Canc. OFF)	NR	4.7[4,5]	**-0.5 (Canc. OFF)[4,5]**
	IP3 (dBm)	-29[6,7]	-15[7,8]	NR	10.6[4,5]	**7.9[4,5]**
Noise Performance		3.4-5.8 dB Noise Figure	4.3-6.3 dB Noise Figure	60 dB SNDR	330 μV_{rms} (Output-referred)	**32.6 dB SNDR**
Power (mW)		116-147[9]	280-340[9]	453	47	**25 (8 VTCs) 12 (TDC) 3 (Clock) 40 (Total)**
Area (mm²)		2.25[9] 1.44 (active)	23.4[9]	4.42 0.29 (active)	0.57	**0.82 0.31 (active)**

NR: Not reported; NA: Not applicable; [1]Visually derived from slide 35 of ISSCC 2019 presentation; [2]Raw bandwidth calculated for 3Gb/s 64QAM; [3]Assuming RF front-end at carrier frequency of $\frac{(N-1)}{2*TTD\ Range}$; [4]1-element; [5]BB RX only; [6]Receiving angle; [7]IIP3= OIP3-Conversion Gain; [8]Calculated for receiving angle when signal-to-blocker incidence difference is 90°; [9]RF included, NO ADC.

Figure 10.8.6: Comparison of the 4-element SSP with the state-of-the-art.

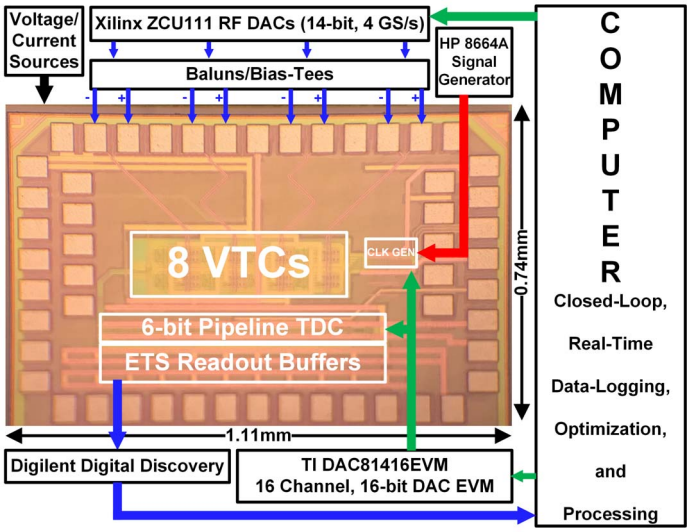

Figure 10.8.7: Die micrograph in 65nm CMOS and test setup.

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