A 66.97pJ/bit, 0.0413mm^2 Self-Aligned PLL-Calibrated Harmonic-Injection-Locked TX with >62dBc Spur Suppression for IoT Applications

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***Abstract*—Digital-intensive ultra-low-power (ULP) wireless transmitters (TX) employing harmonic injection locking suffer from large close-in reference spurs that violates the TX spectral mask. This paper presents a self-aligned type-I PLL in conjunction with harmonic injection locking to achieve significantly improved spur performance at ULP for sub-GHz IoT TXs. The on-chip type-I PLL calibrates the phase error in the ring oscillator (RO) in real time and avoid large spurs induced from the frequency deviation in the harmonic injection-locked technique through the proposed twin-T notch filter in the feedback loop. Implemented in 180nm CMOS process, the proposed frequency translating TX occupies an active area of only 0.0413mm^2 with -14dBm output at 915MHz. We report the lowest power consumption with 3X improved energy-efficiency while consistently achieving >62dBc spur suppression. The TX also supports OOK modulation with an average power consumption of 200.9μW only at 3Mb/s data rate achieving 66.97pJ/bit energy efficiency.**

***Keywords*— Ultra-low-power transmitter, spur suppression, self-aligned PLL, injection-locked TX.**

I. Introduction

Embedding wireless connectivity into billions of internet-of-things (IoT) and biomedical application devices has created the need for long-lasting sub-GHz wireless transmitters (TX). However, the constrained battery capacities put stringent design requirements on the wireless TX which requires not only high energy-efficiency (pJ/bit) but also low spurious emissions with minimum number of external off-chip components.

Recent ULP TXs have demonstrated either reduced power consumption at the cost of poor spur suppression [1], or good spur suppression performance (<50dBc) but with increased hardware complexity and power consumption [2-4]. Though TXs using frequency translation through harmonic injection-locked ring oscillators (RO) have been shown to overcome the constraints of limited power consumption [5], they too suffer from large close-in reference spurs making them unsuitable for IoT applications in ISM bands. In [1], injection-locked RO was demonstrated with low-power wireless TX that combines phase-shifted low-frequency clocks for 401MHz carrier generation. However, the demonstrated architecture has limited spur suppression even at the fundamental injection locking and is limited to low combining ratios. In [2], an external FPGA was used in feedback to calibrate the RO avoiding the need for injection locking, but large power and integration cost due to off-chip components make it infeasible to integrate in the millimeter-scale IoT TXs. In [3], harmonic injection locking was used with digital DAC-based frequency calibration to compare two consecutive RO outputs. However, the DAC quantization noise, precision, and mismatch largely limits the oscillator calibration performance. A harmonic suppression technique using pulse-generators was also proposed in [4], but the need for differential configuration and stringent matching requirements limits its adoption in sub-GHz IoT TXs.

To address these issues, this work minimizes the spurious emission while achieving ULP operation by correcting phase errors from injection locking with a self-aligning type-I PLL in conjunction with a harmonic injection-locked ring-oscillator (HILRO). Initially, since the phase difference between two inputs of the phase detector is quite large, the proposed PLL tries to reduce the phase error while also bringing the RO frequency close to the injection-locked frequency. After this coarse acquisition process, the injection-locked technique self-starts the fine tuning process by drawing or injecting current into the RO capacitive load. This process ends as the difference between oscillator and the injection signal approaches zero. The alignment between two paths (PLL and HILRO) is achieved after the coarse and fine tuning processes are over. After the phase error correction, the TX performs frequency translation using an edge combining power amplifier (ECPA) at 915MHz. The proposed TX with single-ended implementation in 180nm CMOS realizes minimal power consumption and cost, and high energy-efficiency compared to the state-of-the-art.

The rest of the paper is organized as follows. Section II briefly compares the proposed architecture to state-of-the-art. Section III illustrates the proposed TX architecture and circuit design techniques. Section IV presents the measurement result, followed by conclusions in Section V.

II. Brief Background

As shown in Fig. 1(a), a conventional TX has all blocks operating at the carrier frequency leading to relatively large power consumption for ULP TXs. In contrast, the HILRO architecture shown in Fig. 1(b) uses low-frequency synthesis to upconvert the baseband signal to RF which successfully minimize the number of blocks operating at high frequency. Fig. 1(c) shows the fundamental concept behind the harmonic injection technique that while energy-efficient also leads to significant spur generation. The harmonic injection locking phenomenon locks a free-running oscillator in the TX to the Nth harmonic of the injected reference signal generated by a narrow periodic pulse generator. When injection-locked, the oscillator tracks the reference clock every N cycles and runs

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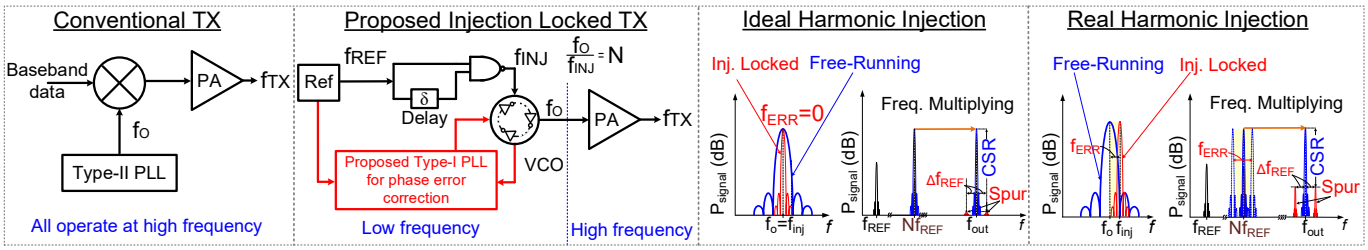

Fig. 1. (a) Conventional TX architecture and (b) proposed harmonic injection-locked ring-oscillator (HILRO) based TX with phase-error correction. Frequency response of harmonic injection-locked TX for (c) ideal and (d) real cases.

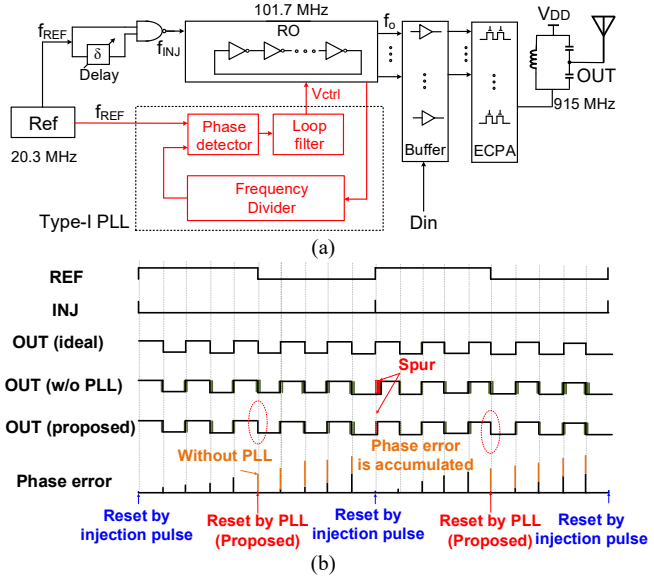

Fig. 2. (a) Proposed HILRO TX with self-aligned PLL, and (b) timing diagram comparing ideal, conventional and proposed TX outputs.

freely for N-1 cycles. In practice however, any mismatch in the oscillator free-running frequency (f_O) and the injection frequency (f_{INJ}) create large frequency errors (f_{ERR}) resulting in unwanted spurs around the TX output significantly degrading the TX spurious performance, as shown in Fig. 1(d). These are especially harder to filter in the harmonic injection-locked transmitters. In absence of any real-time error correction, higher-order harmonic injection results in large frequency deviations and oscillator drifts that can easily exceed the lock range. Real-time calibration loop is thus needed to correct these phase errors [5].

We propose a self-aligned type-I PLL based technique for spur suppression in HILRO. The type-I PLL has only one integrator contributed by the VCO. Hence additional nulling resistor and capacitor are not required resulting in area savings when compared to type-II PLLs. Further, the type-I PLL does not need a charge pump saving area and reducing loop noise. Nevertheless, static phase-error results in higher reference spur due to the ripple on the VCO voltage control line (Vctrl) [6]. To mitigate this, we employ a twin-T notch filter (Section III) within the PLL loop to dampen the undesired frequency components beyond the initial dampening provided by the type- I PLL. The proposed architecture thus overcomes the trade-offs between bandwidth, spur, and power consumption.

III. PROPOSED DESIGN OF HILRO TX

Fig. 2(a) shows the proposed self-aligned type-I PLL with a 9-stage HILRO for real-time phase-error correction and spur suppression. The HILRO output is applied to a NAND-based ECPA. The multi-phase outputs from the 9-stage RO at 101.7MHz are combined by the ECPA to generate 915MHz at the TX output. Unlike LC-VCO based injection-locked PLL that needs to overcome the race condition between the injection path and the PLL loop [5], the RO is inherently immune to the race problem due to its multi-phase output. It also doesn't require a separate transformer to provide multiple injection points as in the LC tank. Therefore, the injection phase to the RO is designed to be different from the PLL feedback path to decouple the race condition that is common in LC-VCO based injection-locked PLLs. An external tapped-capacitor matching network translates the TX output impedance to 50Ω considering all the parasitic effects of the wirebond and the QFN package.

Fig. 2(b) shows the timing diagram of the proposed HILRO TX. Due to the mismatch of each delay cell in the RO, the phase error across the RO is accumulated. While this results in small frequency deviation between the RO and the injected frequency for fundamental injection locking, its effect is amplified for the harmonic injection-locked technique due to its limited locking range that can cause the RO to not lock. Using the PLL resets the phase error between two injection points thus not only minimizing the spur but also the chance to not lock due to frequency deviations. A 20.3MHz external clock source (Ref) feeds into a pulse generator (PG) and the phase detector (PD).

The transistor-level schematic for the proposed TX is shown in Fig. 3. The overall spur contribution at the proposed TX output can be classified as 1) spur due to the injection-locking technique and 2) spur that comes from the PLL loop. The spur due to the injection-locking technique can be expressed as [7]:

$$\mathrm{Spur_{INJ}} = 20\log\left(\mathrm{N}\times\frac{\left|\mathrm{N}\times f_{REF}-f_{o,free-running}\right|}{f_{o,free-running}}\right) \quad (1)$$

where N represents number of harmonics, f_{REF} is the reference frequency, and $f_{o,free-running}$ is the frequency of the free-running oscillator. The term $\left|\mathrm{N}\times f_{REF}-f_{o,free-running}\right|$ in (1) is minimized by the proposed type-I PLL and thus $\mathrm{Spur_{INJ}}$ is suppressed. However, PLL itself also contribute spur from the control line ripple that occurs at the TX output offset by f_{REF}. The PLL spur can be quantified as [8]:

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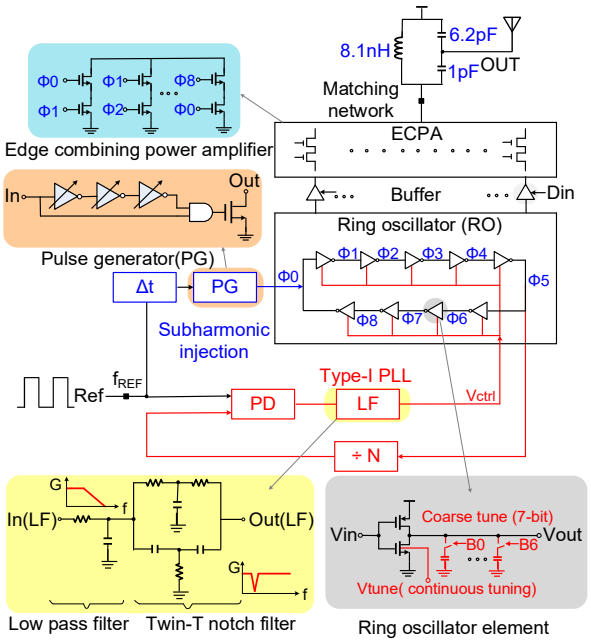


Fig. 3. Block schematics of the proposed HILRO TX.

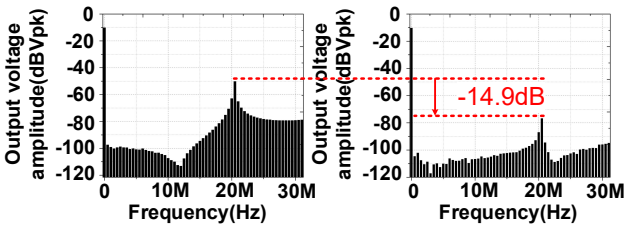


Fig. 4. Simulated PLL control voltage frequency response without and with notch filter.

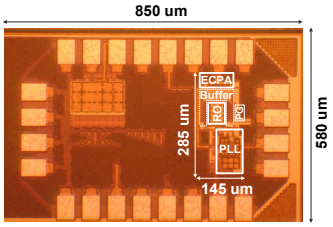
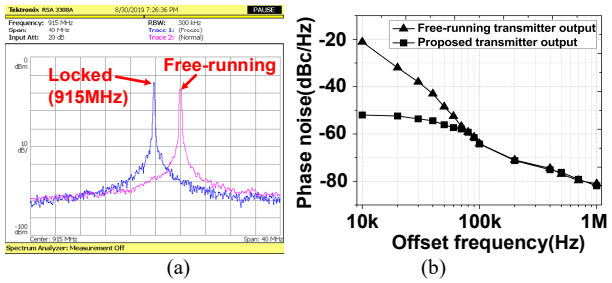


Fig. 5. Chip micrograph of the proposed HILRO TX.

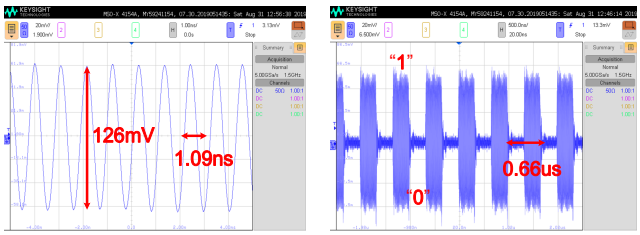
$$\mathrm{Spur}_{\mathrm{PLL}} = 20\log\left(\frac{K_{VCO}\times\Delta V_{ctrl}}{2\pi\times f_{REF}}\right) \quad (2)$$

where K_{VCO} is the VCO gain and ΔVctrl is the voltage variation of the output voltage after the loop filter. In the proposed design, f_{REF} and K_{VCO} are kept constant and the spur magnitude mainly depends on ΔV_{ctrl}. In addition to the first-order low pass RC filter, the twin-T filter is introduced to minimize the ΔV_{ctrl}. The null frequency of the proposed twin-T notch filter is set to 20.3MHz (equal to f_{Ref}) by the combination of a high-pass and a low-pass filter so that the spur from the VCO control line is further suppressed. Behavioural modelling of the PLL in MATLAB including the notch filter achieved a bandwidth of 7.5MHz with 12µS settling time. Fig. 4 further shows 14.9dB suppression is achieved after employing the notch filter. Each RO delay cell has 7-bit coarse tuning with forward body-biased fine tuning



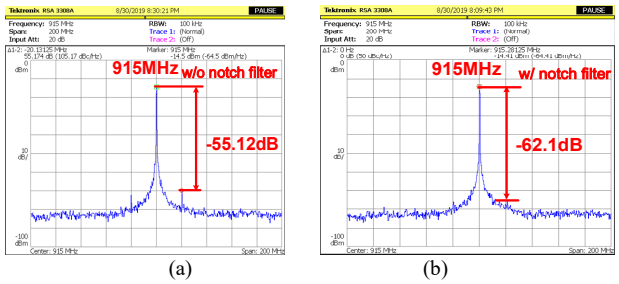
(a) (b)

Fig. 6. (a) Measured transient output waveform, and (b) measured transient output applying 3Mb/s OOK modulation.



(a) (b)

Fig. 7. (a) Measured transient output waveform, and (b) measured transient output applying 3Mb/s OOK modulation.



(a) (b)

Fig. 8. Measured output spectrum (a) without and (b) with notch filter.

that sets the RO frequency and the tuning range within the ISM band range. The coarse tuning is designed to change the loading capacitor of each delay cells to calibrate the RO frequency to overcome the PVT variations. A tunable delay (Δt, Fig. 3) is placed before the PG to ensure the correct injection locking and accommodate a finite phase error in the injection locking path [9].

IV. MEASUREMENT RESULTS

The proposed HILRO TX was prototyped in 180nm CMOS occupying a core area of only 0.0413 mm^2. Fig. 5 shows the die micrograph of the PCB-mounted IC. Fig. 6(a) shows the measured spectrum for the proposed TX in free–running and locked mode demonstrating a 4MHz lock range while delivering an output power of -14dBm. The phase noise of the free-running and locked TX output is also shown in Fig. 6(b). The close-in phase noise is suppressed within the 80kHz bandwidth. For modulation testing, on-off keying (OOK) signal is generated with bit pattern of 1010101010. Fig. 7(b) demonstrates the measured time-domain output signal at a data rate of 3Mb/s. The measured power consumption. with OOK modulation is 200.6 µW . Fig. 8(a)(b) shows the improved spur suppression in the proposed TX with the phase error correction over 200MHz at the center frequency of

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Table 1. Performance summary and comparison with state-of-the-art sub-GHz TX

	[1] JSSC'11	[10] JSSC'14	[11] JSSC'17	[12] ISSCC'17	[2] TMTT'18	This Work
Frequency (MHz)	401	402	401-428	915	918	915
Spur suppression method	Open-loop	Mismatch-free IL freq. multiplier	Digital Freq. Calibration	None	Off-chip FPGA	PLL
Key components	RO + ECPA	IL freq. multiplier + PA	Frac-N PLL w/ RO + ECPA	Power LC oscillator	FPGA + RO + ECPA	Type-I PLL w/ RO + ECPA
P_{OUT} (dBm)	-17	-16	-13	-1.64†	-10/-15	-14
Modulation	BFSK	OOK	BFSK/QPSK	Sparse PPM	BFSK	OOK
Carrier-to-spur ratio (dBc)	44.4	52.2	Not reported	Not reported	Not reported	62.1
P_{DC} (µW)	90	215	4060/4080	2000	935/620	258.6(Peak) 200.9 (OOK)
Data rate (kb/s)	200	250	550/11000	30.3	3000	3000
Energy efficiency (pJ/bit)	450	860	7420/370	66010	311/200	66.97
FoM[1](nJ/(bit*mW))	22.5	34.238	148.4/7.4	96.28	3.1/6.325	1.674
Area (mm^2)	0.04[2]	Not reported	0.643[2]	2.676[3]	0.4528[2]	0.0413[2]
`Tech. (nm)	130 (CMOS)	65 (CMOS)	180 (CMOS)	180 (CMOS)	180 (CMOS)	180 (CMOS)

†Estimated by the data provided in [9]; [1]FOM= P_{DC}/(Data Rate × P_{OUT}); [2]Active area; [3]The area includes system interfaces, RX, baseband controller and timer.

915MHz. Based on the harmonics allocation, the nearest spur will be 20.3 MHz (894.7MHz and 935.3MHz) away from the main tone. The proposed notch filter improves the spur suppression by 7dB with the PLL locked. The spur suppression without the PLL couldn't be measured independently in the current setup. The reference spur with and without the notch filter was measured from 4 samples. The worst case is 62.1dBc, and the best case is 63.7dBc demonstrating the effectiveness of the proposed technique.

Table 1 compares the proposed work with state-of-the-art standard-compliant sub-GHz TXs. The entire TX consumes only 258.6µW with 114.46µW for ECPA, 60.3µW for RO, 5µW for PG, 67.5µW for buffers, and 10.86µW for PLL comprising the clock divider and the PD. We report the lowest power consumption with 3X improved energy-efficiency while consistently achieving >62dBc spur suppression.

V. CONCLUSION

An ULP 915MHz TX with improved spur suppression is proposed for sub-GHz IoT applications. A digital intensive architecture is proposed with a type-I PLL to correct the phase-error due to injection-locking while also simultaneously achieving high energy-efficiency at low-cost. The PLL loop filter includes a twin-T notch filter to suppress any voltage ripple and consequently, suppress the PLL induced spur. The active power consumption without any modulation is only 258.6µW with -14dBm output power. Under OOK modulation, a 3MB/s data rate is demonstrated with an energy-efficiency of 66.97pJ/bit. The average power consumption can be further minimized with aggressively duty-cycling. The proposed TX will thus be suitable for sub-GHz low-power IoT wireless sensor network applications.

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